Embedded USB2 (eUSB2) Physical Layer Supplement to the USB Revision 2.0 Specification

Revision 1.0

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1 Preface

1.1 *Scope of this Revision*

This supplement defines eUSB2 PHY layer requirement and signaling attributes. Protocol behavior which is not explicitly called out in this document shall remain the same as defined in USB Revision 2.0 specification.

1.2 *Revision History*

Revision Number	Date	Description
1.0	1 August, 2014	Initial release

2 Introduction

2.1 *Motivation*

The success of USB2.0 technology has enjoyed wide adoption in almost every computing device, with tremendous ecosystem support not only in terms of device choice to support various platform features, but also in terms of technology development with well-established hardware IP portfolios and standardized software infrastructure. It is foreseeable that the great asset of USB2.0 technology will continue to benefit the ecosystem for years to come.

As power efficiency becomes increasingly critical in today's computing devices, there is a need for IO technology to be optimized for both active and idle power. USB2.0 technology, originally optimized for external device interconnect, is primed to be enhanced for inter-chip interconnect such that the link power can be further optimized.

Meantime, silicon technology continues to scale. Device dimensions are getting smaller and therefore more devices can be packed onto a single integrated chip. However, the device reliability challenge arising from the densely packed transistors has become more profound. The manufacturing cost for an advanced process technology to support 3.3V IO signaling has grown exponentially. A low voltage USB2.0 solution is therefore required to address the gap.

In summary, eUSB2 is introduced to address the following:

1. IO Power Efficiency
   - Improve both the link active and idle power efficiency.
2. Process scalability
   - Provide a low voltage USB2.0 PHY solution to eliminate 3.3V IO signaling requirement, which allows the process technology to continue to scale for many generations to come.
3. Implementation simplicity
   - The PHY analog content is reduced. Digital mechanisms are employed for PHY functionality, for example, device disconnect detect.
4. Support both USB2.0 inter-chip and out-of-the-box devices
   - Though eUSB2 and USB2.0 are not electrically compatible, a mechanism is defined for eUSB2 to support standard USB2.0 devices.

Table 2-1 tabulates the key attributes of eUSB2 technology in comparison to other USB interfaces.

Table 2-1: Comparison of Various USB Interfaces

	USB2	**IC-USB**	**HSIC**	**ULPI**	**eUSB2**
Interface Pin (SoC view)	2-pin	2-pin	2-pin	12-pin	2-pin
Supported data rate	low-speed, full-speed and high-speed	low-speed and full-speed	high-speed	low-speed, full-speed and high-speed	low-speed, full-speed and high-speed
Connectivity	Inter-chip and out-of-the-box	Inter-chip	Inter-chip	Inter-chip	Inter-chip and out-of-the-box USB2.0 connectivity through repeater

	USB2	**IC-USB**	**HSIC**	**ULPI**	**eUSB2**
Signaling Voltage Requirement	Max 3.3V	Multiple voltage classes, from 1V to 3.3V	1.2V	Vendor specific. Typically 1.8V and 3.3V	Max 1V
Recommended trace length support	Long	short	short	short	Medium to long

2.2 *eUSB2 PHY Feature*

eUSB2 is fully compliant to USB2.0 layer architecture with the following features and characteristics:

- Supports high-speed, full-speed, and low-speed operation.
    - High-speed:
        - Low voltage differential signaling
    - Low-speed/Full-speed:
        - Single-ended digital CMOS 1V signaling, compliant to JEDEC standard [JESD8-14A.01].
- Supports selected single speed configuration in native mode.
- Supports USB2.0 operation based on repeater architecture.
- Supports link power management LPM-L1 (L1) and Suspend (L2).
- Supports UTMI/UTMI+ implementation. Note that implementations based on UTMI/UTMI+ may vary. In the rest of the specification UTMI* is quoted as a reference to describe the interface between the protocol layer and the eUSB2 PHY.
- Supports register access protocol (RAP) for eUSB2 device or repeater configurations.
- Fully compliant to [USB2.0] base spec at the protocol layer.
- No change to USB2.0 software programming model.

Not compatible with the physical layer defined by [USB2.0].

- Not compatible with standard USB2.0 connectors defined by [USB2.0] and its derivatives.

Shown in Figure 2-1 is a description of eUSB2 scope. An implementation that supports UTMI* as the standard interface between the protocol layer and the physical layer is used as an example.

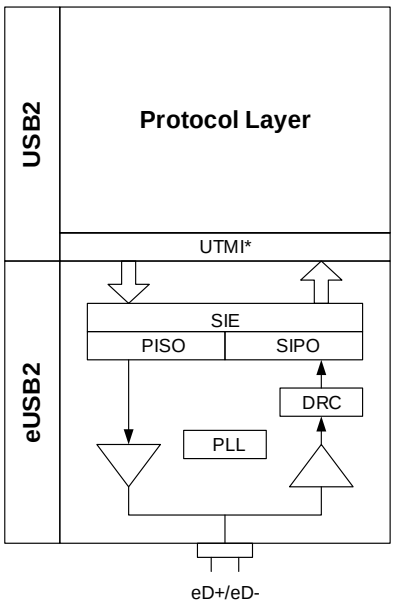


Figure 2-1: eUSB2 Under USB2.0 Layer Architecture

2.3 *eUSB2 Modes of Operation*

eUSB2 supports two modes of operation: native mode and repeater mode.

Native mode refers to a host port and a device port both implementing a eUSB2 PHY and communicating based on eUSB2 signaling. Native mode eUSB2 is used for inter-chip interconnect. Single speed configuration is allowed in native mode.

Repeater mode refers to a eUSB2 port communicating with a USB2.0 port through a repeater that translates between eUSB2 signaling and USB2.0 signaling. Repeater mode may also be used between two eUSB2 ports communicating with each other through two repeaters, such a case typically involves applications with USB2.0 receptacles at both sides of the ports.
Example usages of eUSB2 in native mode and repeater mode are shown in Figure 2-2. Note that in Figure 2-3, SoC-1 is only host capable and its eUSB2 repeater only supports host function. SoC-2 is dual role capable, and its eUSB2 repeater supports both host function and peripheral function depending on the usage scenarios.

A eUSB2 implementation on a SoC may support both native mode and repeater mode operation with slight differences in accommodation for repeater operation. This gives the system designer the flexibility to determine the mode of operation of the eUSB2 port on a SoC.

In the specification the following port naming conventions will be used:

- eDSPn: the downstream eUSB2 port of a host/hub in native mode.
- eUSPn: the upstream eUSB2 port of a device in native mode.

- eDSPr: the downstream eUSB2 port of a host/hub in repeater mode.
- eUSPh: the upstream eUSB2 port of the host repeater.
- UDSP: the downstream USB2.0 port of the host repeater.

- eUSPr: the upstream eUSB2 port of a device in repeater mode.
- eDSPp: the downstream eUSB2 port of a peripheral repeater.
- UUSP: the upstream USB2.0 port of a peripheral repeater.

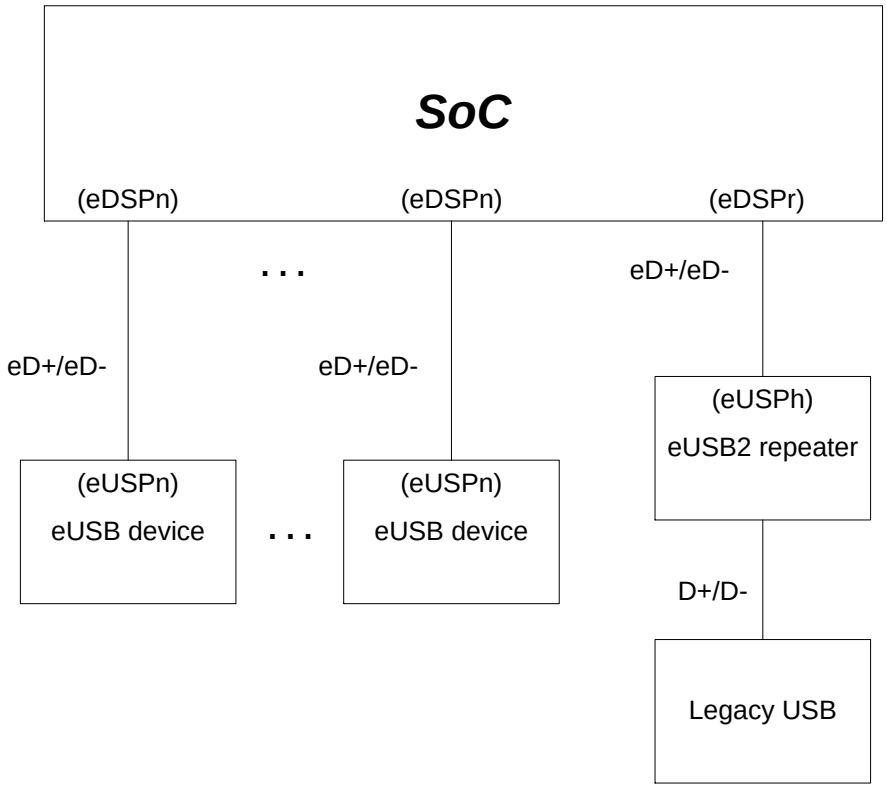


Figure 2-2: Typical eUSB2 Use Cases

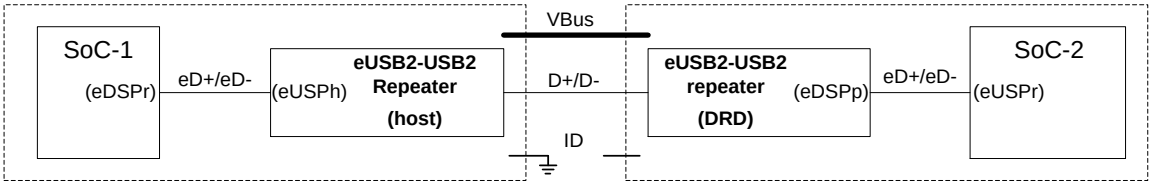


Figure 2-3: Example eUSB2 With Host and Device Side Repeaters

2.4 *Related Documents*

eUSB2 only defines the physical layer. The protocol layer is defined in the [USB2.0] base specification.

The related documents can be found in the following locations:

1. USB-IF website, www.usb.org/developers/

[USB2.0]	Universal Serial Bus Revision 2.0 Specification including ECNs and errata.
[USB2 OTG]	On-The-Go and Embedded Host Supplement to the USB Revision 2.0 Specification.
[BC1.2]	Battery Charging v1.2 Specification

2. ULPI website, http://www.ulpi.org/documents.html

[UTMI+ v1.0] USB 2.0 Transceiver Macrocell Interface Plus(UTMI+) Specification.

3. JEDEC website, www.jedec.org

[JESD8-14A.01] 1.0 V +/- 0.1V (Normal Range) and 0.7 - 1.1 V (Wide Range) Power Supply Voltage and Interface Standard for Non-terminated Digital Integrated Circuits.

2.5 *Terminology*

"Shall" is normative and used to indicate mandatory requirements which are to be followed strictly in order to conform to this standard.

"Should" is normative and used to indicate a recommended option or possibility.

"May" is normative and used to indicate permitted behavior.

"Can" is informative and used to indicate behavior which is possible or may be seen.

The use of "must" and "will" is deprecated for requirements and shall only be used for statements of fact.

2.6 *Acronyms and Terms*

This section lists and defines terms and abbreviations used throughout this specification.

Table 2-2: Acronyms

Acronyms	Terms
Attach	This specification makes a distinction between the words "attach" and "connect". A downstream device is considered to be attached to an upstream port when there is a physical cable between the two
Analog Ping	A analog pulse of differential signal with variable pulse width used by an upstream eUSB2 port in high-speed operation to indicate its presence
BU	Bottom Up
CDP	Charging downstream port
Connect	A downstream device is considered to be connected to an upstream port when it is attached to the upstream port, and when the downstream device has pulled either the D+ or D- data line high through a 1.5 kΩ resistor, in order to enter low-speed, full-speed or high-speed signaling.
D+	USB2 data+ pin
D-	USB2 data- pin
DCP	Dedicated charging port
DRD	Dual role device capable of host function and device function
DSP	Downstream port
Digital Ping	A single-ended digital pulse of various pulse width used in the eUSB2 operation as a ping or an acknowledgement
Downstream	The direction of data flow from the host or away from the host. A downstream port is the port on a hub/repeater electrically

Acronyms	Terms
	farthest from the host that generates downstream data traffic from the hub. Downstream ports receive upstream data traffic
eD+	eUSB2 data+ pin
eD-	eUSB2 data- pin
eDSPn	Downstream eUSB2 port in native mode
eDSPp	Downstream eUSB2 port of the peripheral repeater
eDSPr	Downstream eUSB2 port in repeater mode
ESE1	Extended SE1
eUSPh	Upstream eUSB2 port of the host repeater
eUSPn	Upstream eUSB2 port in native mode
eUSPr	Upstream eUSB2 port in repeater mode
FS	Full-speed
HS	High-speed
LPM	Link Power Management
LS	Low-speed
Lx	Link power management states, includes both L1 and L2.
L1	LPM-L1
L2	Suspend
PVTB	Presence verification topdown bottomup
RAP	Register Access Protocol
Redriver	Non-retiming repeater
Retimer	Retiming repeater
Repeater	General term of a bridge. In this specification, it refers to non-linear eUSB2-USB2 redriver.
SC	Session controller
SCD	Session controller for USB DRD
SCH	Session controller for USB host
SCP	Session controller for USB peripheral
SCM	Start of Control Message
SDP	Standard downstream port
SE0	Single Ended Zero
SE1	Single Ended One
SoC	System-on-chip
TD	Top Down
Upstream	The direction of data flow towards the host. An upstream port is the port on a device electrically closest to the host that generates upstream data traffic from the hub/repeater. Upstream ports receive downstream data traffic.
UDSP	Upstream USB2.0 port of the peripheral repeater
UUSP	Downstream USB2.0 port of the host repeater
USB OTG	USB On-the-go
USB session	The lifetime of a USB port in connected state
UTMI*	The interface between the protocol layer and the eUSB2 PHY. The asterisk indicates that this term includes both UTMI v1.05 and UTMI+ v1.0.
Walk-up port	Ports which have physical connectivity through the connector

3 eUSB2 PHY Architecture and Operation

This chapter describes the eUSB2 PHY architecture and its operation. Although the focus is on native mode, most of native mode operation also applies to repeater mode.

3.1 *PHY Architecture*

A conceptual block diagram of the eUSB2 PHY is shown in Figure 3-1. It supports three data rates defined by USB2.0. A differential transceiver and a low power squelch detector is needed for data transfer at high-speed. Two-pairs of single-ended CMOS buffers are employed to carry out low-speed/full-speed data transfer, control signaling during initialization and link power state transitions. In addition, a host port has a pair of pull-down resistors intended to hold the bus to ground during power-up or when the link is idle. A device port also has a pair of pull-down resistors at eD+ and eD- to hold the bus to ground when the host is not present.

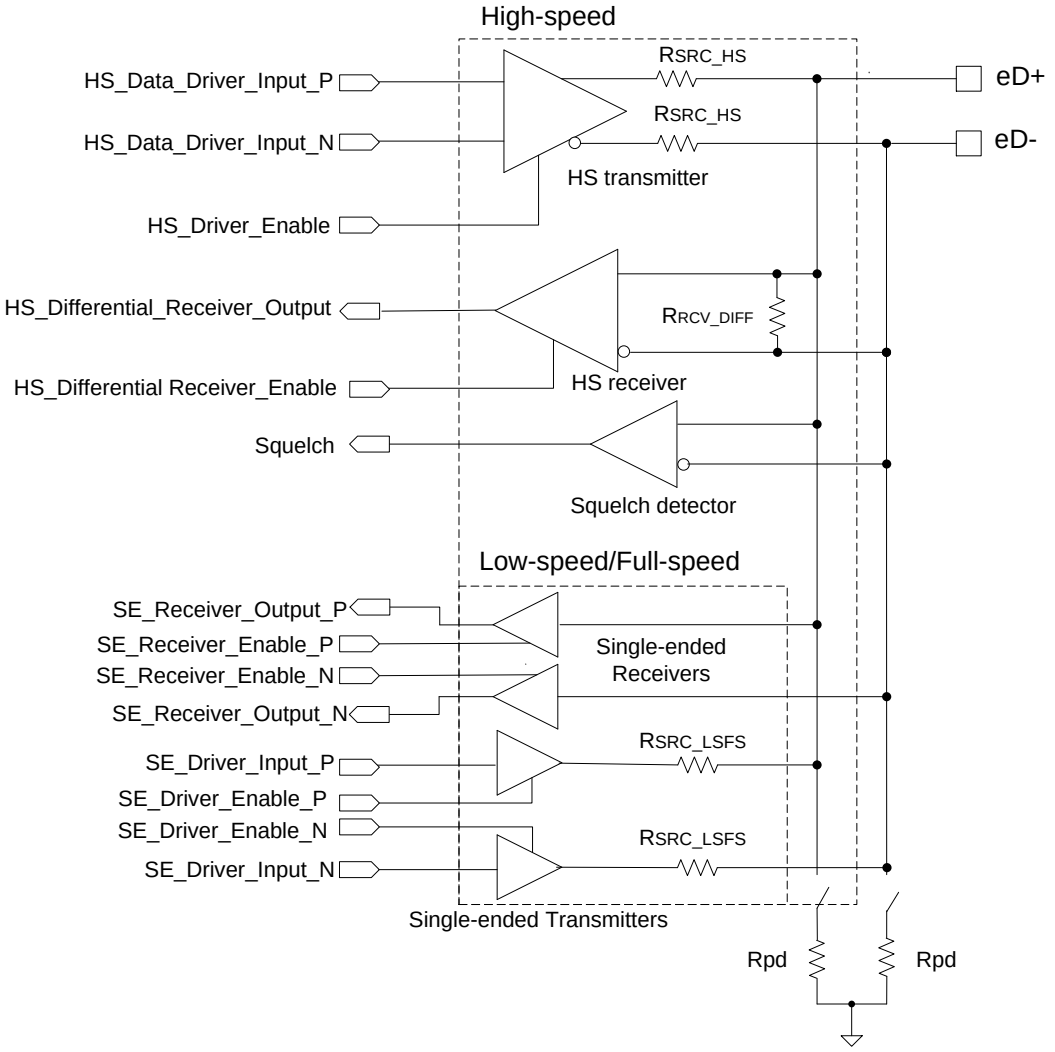


Figure 3-1: eUSB2 Physical Layer Block Diagram

A eUSB2 implementation shall contain the following building elements:

- A port shall implement two tristate-able pull-downs, R_{PD}.
- A low-speed/full-speed eUSB2 port is fully digital. A low-speed/full-speed transceiver shall meet the following requirements:

  - The port shall implement a pair of low-speed/full-speed transmitters.
  - The port shall implement a source termination at its transmitter.
  - The port shall implement a pair of low-speed/full-speed receivers.
- A high-speed transceiver shall meet the following requirements:
  - The port shall implement an analog transceiver for low swing differential signaling.
  - The port shall employ embedded clocking compliant to [USB2.0].
  - The port shall implement a squelch detector.
  - The port shall implement a source series termination at its transmitter.
  - If enabled, the port shall implement a differential receiver termination with the center tap capacitance to ground. Note that the differential receiver termination not to ground is to avoid overloading the SE (Single-ended) transmitter in HS operation when a control message may be issued during HS idle. Refer to Section 3.5 for control message definition.
  - The default receiver termination shall be enabled in repeater mode, and disabled in native mode. A downstream port may alter the termination scheme during Reset. Refer to Section 3.5 for the details.

3.2 *Bus State and Signaling*

The bus state of eUSB2 is similar to USB2.0 with the main exception that the idle state of eUSB2 bus at LS/FS and L1/L2 is always SE0, rather than idle J.

3.2.1 Low-speed/Full-speed Bus State and Signaling

In order to differentiate low-speed from full-speed signaling, all low-speed signaling is the inverse of full-speed (eD+ and eD- are swapped), with the exception of control message signaling. Table 3-1 defines the low-speed/full-speed bus states and their associated signaling.

Table 3-1: eUSB2 Low-speed/Full-speed Bus State Representations

Bus State		**Signaling Levels**	
		At the source[1]	**At the sink[2]**
Logic ‘1’		> V_{OH}(min)	> V_{IH}(min)
Logic ‘0’		< V_{OL}(max)	< V_{IL}(max)
Single-ended 0 (SE0)		Logic ‘0’ at eD-; Logic ‘0’ at eD+	
Single-ended 1 (SE1)		Logic ‘1’ at eD-; Logic ‘1’ at eD+	
Data J state[3]:	FS	Logic ‘0’ at eD- Logic ‘0’ at eD+	
	LS	Logic ‘0’ at eD- Logic ‘0’ at eD+	
Data K state[3]:	FS	Logic ‘1’ at eD- Logic ‘0’ at eD+	
	LS	Logic ‘0’ at eD- Logic ‘1’ at eD+	
L0 Idle/L1/L2 state		SE0[4]	
Resume	FS	Logic ‘1’ at eD-	
	LS	Logic ‘1’ at eD+	
Remote Wake	FS	Logic ‘1’ at eD+	
	LS	Logic ‘1’ at eD-	
Start-of-Packet(SOP)		transition from SE0 to data K	

End-of-Packet(EOP)	FS	3 UIs of logic '0' at eD- 1 UI of logic '1', 1UI of logic '0', then 1 more UI of logic '1' at eD+
	LS	3 UIs of logic '0' at eD+ 1 UI of logic '1', 1UI of logic '0', then 1 more UI of logic '1' at eD-
Reset		SE1 followed by Reset control message
Connect (device drive eD+ or eD- upon power-up)	HS/FS	R_{PD} at eD-; Logic "1" at eD+
	LS	Logic "1" at eD-; R_{PD} at eD+

Note 1: Source is defined at the pin level of a transmitting port.
Note 2: Sink is defined at the pin level of a receiving port.
Note 3: Data states J and K are only valid during packet transmission and high-speed detection.
Note 4: Driven through R_{PD}.

3.2.2 Low-speed/Full-speed Idle State Transition

Low-speed/Full-speed idle state (SE0) is maintained by the pull-down resistors implemented at a downstream port (Refer to R_{PD}, Section 6.3). To ensure a swift transition to idle state, the port shall drive the bus to SE0 and then disable its transmitters to allow the pull-down resistor to hold SE0. The port shall drive a non SE0 state to SE0 within $T_{SE0\_DR\_LSFS}$ defined in Table 6-15 .

3.2.3 High-speed Bus state and Signaling

High-speed bus states of J and K are maintained by driving low swing differential voltage on eD+ and eD- during terminated and un-terminated conditions. Figure 3-2 defines the high transmitting signals at eD+ and eD-, each is denoted as $V_{TX(eD+)}$ and $V_{TX(eD-)}$. The differential signal $V_{TX\_DIF\_TERM}$ (during terminated) or $V_{TX\_DIF\_UNTERM}$ (during un-terminated) and the common mode signal V_{TX_CM} are then represented by the following:

$$V_{TX\_DIF} = V_{TX(eD+)} - V_{TX(eD-)}$$

$$V_{TX\_CM} = \frac{V_{TX(eD+)} + V_{TX(eD-)}}{2}$$

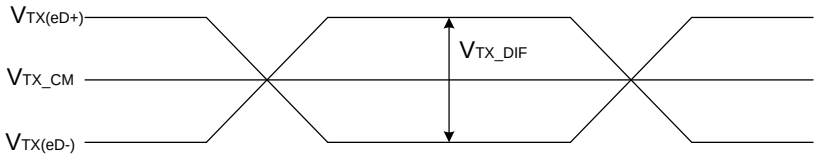


Figure 3-2: High-speed Differential Signal Representations

Accordingly, the differential and common mode signals at the receiving port can be similarly represented by the following equations:

$$V_{RX\_DIF\_UNTERM} = V_{RX(eD+)\_UNTERM} - V_{RX(eD-)\_UNTERM}$$

$$V_{RX\_DIF\_TERM} = V_{RX(eD+)\_TERM} - V_{RX(eD-)\_TERM}$$

$$V_{RX\_CM} = \frac{V_{RX(eD+)} + V_{RX(eD-)}}{2}$$

Table 3-2: eUSB2 High-speed Bus State Representations

Bus State		At the source	At the sink
Differential '1'	Terminated	$V_{TX\_DIF} > V_{TX\_DIF\_UNTERM}$(min)	$V_{RX\_DIF} > V_{RX\_DIF\_SENS}$(min)
	Unterminated	$V_{TX\_DIF} > V_{TX\_DIF\_TERM}$(min)	
Differential '0'	Terminated	$V_{TX\_DIF} < -V_{TX\_DIF\_UNTERM}$(min)	$V_{RX\_DIF} < -V_{RX\_DIF\_SENS}$(min)
	Unterminated	$V_{TX\_DIF} < -V_{TX\_DIF\_TERM}$(min)	
Squelch state		NA	AC: $V_{RX\_DIF} < V_{SQUELCH\_DIF}$(min) $V_{RX\_DIF} > -V_{SQUELCH\_DIF}$(min)
Data J state:		Differential '1'	
Data K state:		Differential '0'	
L0 idle/L1/L2 state		SE0	
Start-of-Packet(SOP)		Same as USB2.0	
End-of-Packet(EOP)		Same as USB2.0	

3.2.4 High-speed Idle State Transition

High-speed idle state is maintained by the pull-down resistors implemented at a downstream port. To ensure a swift transition to idle state, the port shall drive the bus to SE0 at the end of EOP before disabling its transmitters. The port shall drive a non SE0 state to SE0 within $T_{SE0\_DR\_HS}$ defined in Table 6-15 depending on its mode of operation.

3.2.5 High-speed Squelch Operation

The squelch detector is used by the port to detect high-speed line activity. It is also used by the upstream port as one of the conditions to control its single-ended receiver.

- A port receiving high-speed data may optionally disable its single-ended receivers in order to preserve the electrical characteristics of its high-speed receiver.
- An upstream port shall turn on its single-ended receiver in anticipation of a control message (refer to section 3.5) from the host when the link is in squelch state. Note that this does not apply to a eUSB2 upstream port in peripheral repeater mode.

3.3 *Single-ended (SE) Signaling*

eUSB2 employs SE signaling for low-speed/full-speed packet transmission in L0. The SE signal is also used for interactions between the two ports. Interactions include connect, reset, resume, remote wake, high-speed detection and control message. The interpretation of the SE signals depends on the link state, and the start of the SE signal.

- If it is the start of a FS USB packet (SOP), eD- shall be used to transmit the SYNC pattern and packet data, while eD+ shall be logic '0' maintained through R_{PD}. If it is a LS SOP, eD+ shall be used to transmit the SYNC pattern and packet data while eD- shall be logic '0' through R_{PD}.

- For the case of FS USB end of packet (EOP) eD+ shall be used to transmit EOP while eD- shall be logic '0' maintained through R_{PD}. LS EOP shall use eD- to transmit EOP while eD+ shall be logic '0' through R_{PD}.

The SE signal timing is illustrated in Figure 3-3

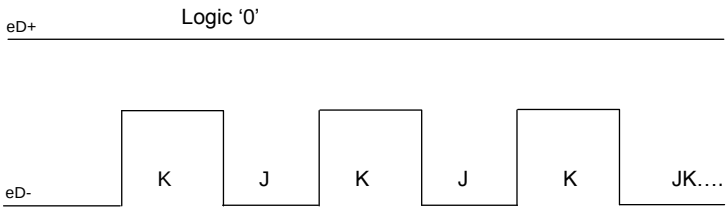


Figure 3-3: FS SOP

- If it is the start of a control message (SCM), a downstream port shall drive an SE1 pulse for the duration of T_{CM_UI} (during L0) or $T_{CM\_SE1\_Lx}$ (during L1/L2) as an indication to start a control message. It shall then follow with a control message encoded by the number of pulses at eD- during T_{CM_ACTIVE} window where eD+ is logic '1'. Refer to section 3.5 for a more detailed description.

Note that the skew of the SE1 rising edge shall be controlled such that in high-speed operation, an SE1 will not be perceived as the beginning of high-speed SYNC.

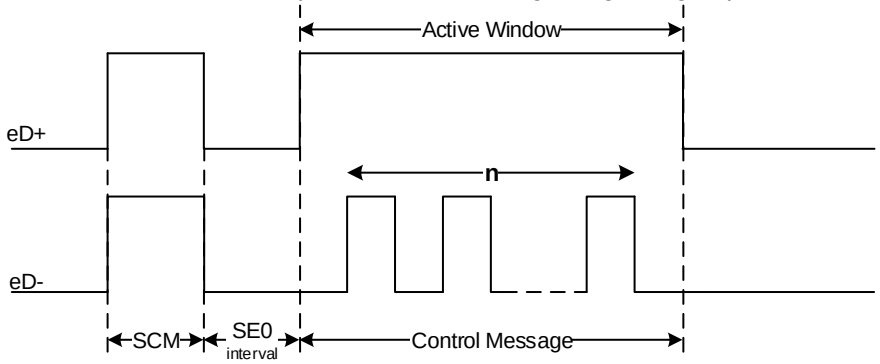


Figure 3-4: SE1 as Start of Control Message

The other usage of SE signaling is for host and device interactions during power-up, reset, suspend, resume and remote wake. Under these conditions, the host and device interact with each other bi-directionally through eD+ and eD-.

3.3.1 Extended SE1

Except for SCM representation, an extended SE1 (ESE1), shown in Figure 3-5, is also defined and used under various circumstances for a port to announce an event of either disconnect or re-connect. The timing of ESE1 is specified such that it shall survive any bus contention without corruption.

- An ESE1 is defined with SE1 duration of T_{EXTSE1}.
- A port shall monitor the line state at eD+/eD- before attempting ESE1 transmission.
- When directed, a port shall transmit ESE1 regardless of the state of eUSB2. Note that ESE1 is defined to survive contention with any other signals in eUSB2.
- When directed, a port may also transmit ESE1 under recovery operation to resolve an unrecognizable eUSB2 bus event. Note that circumstances exist where and unexpected condition is detected that may result in undefined port behavior. Under this condition, a

port may transmit an ESE1 as an attempt to terminate the current USB session and start a new USB session. A port may attempt to start a new USB session no more than three times. If it fails to establish a USB session on the third retry, a downstream port shall disable the port and an upstream port shall enter suspend.

The following is a list of ESE1 definition. Refer to Section 3.7 and 4.2 for details.

- An eDSPn or eDSPr shall transmit an ESE1 upon power on or when directed to start a new USB session. This is referred to as DSP reset announcement. Refer to Section 3.6.2.5 for details.
- An eDSPp shall transmit an ESE1 upon detection of de-assertion of PeripheralEnb. This is also referred to as DSP reset announcement. Note that this applies to only a peripheral repeater using the Bottom-Up configuration. Refer to Section 4.1.3 for details.
- A eUSPn or eUSPr shall transmit an ESE1 upon power on or when directed to perform a connect. This is referred to USP presence announcement. Refer to Section 3.6.2.3 for details.
- A eUSPn or eUSPr shall transmit an ESE1 if directed to perform a graceful device disconnect. This is referred to as device disconnect announcement. Refer to Section 3.6.2.3 for details.
- A eUSPr shall transmit an ESE1 upon detection of de-assertion of PeripheralEnb. This is also referred to as device disconnect announcement. Note that this applies to only a eUSPr connected to a peripheral repeater using the Top-Down configuration.
- A eUSPh shall transmit an ESE1 upon detecting USB2.0 device disconnect. This is also referred to as device disconnect announcement. Refer to Section 3.6.2.3 for details.
- A repeater shall transmit an ESE1 upon power on. This is referred to as repeater presence announcement. Refer to Section 4.2.5 for details.

A port, upon detecting SE1 on the eUSB2 bus, shall declare the reception of ESE1 if the SE1 duration is more than 50us. Note that concurrent ESE1 may exist. Under this situation, the conclusion of ESE1 may likely be asynchronous. If the port concludes ESE1 earlier, it may drive SE0 before switching to pull-down. Contention may occur between SE0 and ESE1. It is recommended that the momentary SE1 discontinuity be ignored.

- A eUSPn or eDSPn, upon declaring ESE1 reception, shall transition to or remain in its initial power on state, and prepare to start a new USB session.
- A eUSPr, eUSPh, eDSPr or eDSPp, upon declaring ESE1 reception, shall transition to or remain in the PVTB state. Refer to Section 4.3 for details.

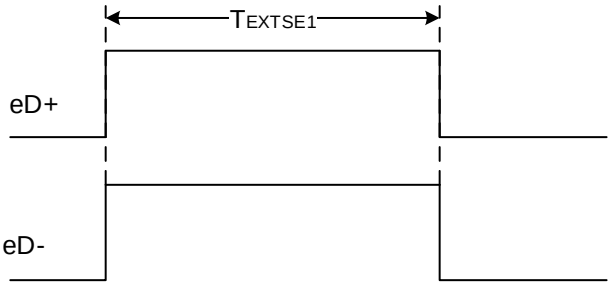


Figure 3-5: Extended SE1

3.4 *Packet Format and Transmission*

eUSB2 shares similar packet format and rules as are defined in USB2.0. This includes SYNC for packet start, EOP as packet end, and the rule for bit-stuffing. This section defines the rules for eUSB2 packet and packet transmission that are different from those defined in USB2.0.

3.4.1 Bit-Stuffing and Data Coding

- eUSB2 shall follow the same bit-stuffing rules defined in USB2.0.
- eUSB2 shall follow the same coding scheme defined in USB2.0.

3.4.2 SYNC and EOP

3.4.2.1 Low-speed/Full-speed Operation

- For FS devices, eUSB2 shall drive the SYNC pattern on eD- while maintaining logic '0' on eD+ through R_{PD}. LS devices shall drive SYNC on eD+ while maintaining logic '0' on eD- through R_{PD}. This is illustrated in Figure 3-6.

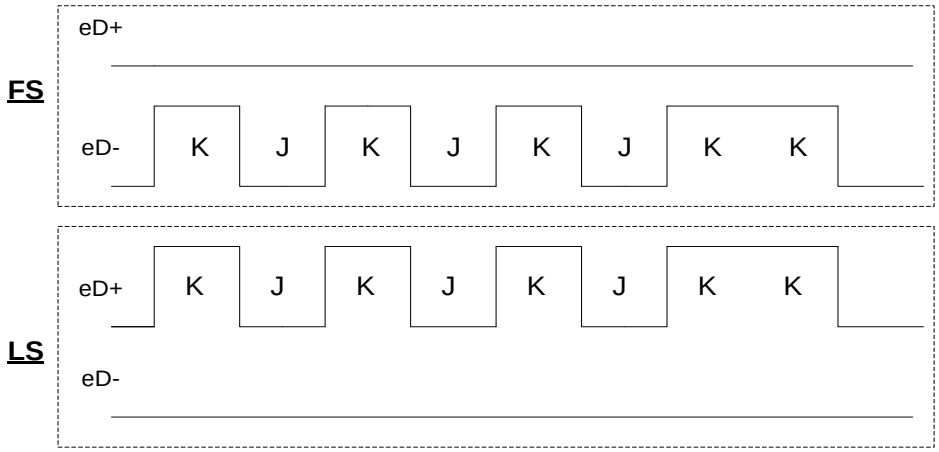


Figure 3-6: FS/LS SYNC Pattern

- A FS eUSB2 EOP, transmitted by an eDSPn, eDSPr, eUSPn or eUSPr, shall be 3 UIs with the first UI of logic '1', followed by the second UI of logic '0', and a third UI of logic '1' at eD+, while eD- is maintained at logic '0' through R_{PD}. This is shown in Figure 3-7. Similarly, a LS EOP, transmitted by an eDSPn, eDSPr, eUSPn or eUSPr, shall be 3 UIs with the first UI of logic '1', followed by a second UI of logic '0', and the third UI of logic '1' at eD-, while eD+ is maintained at logic '0' through R_{PD}. Note that the definition of EOP format is optimized towards repeater mode operation to provide timing support when a eUSB2 LS/FS EOP is converted to a USB2.0 EOP. An example eUSB2 EOP to USB2.0 EOP conversion in repeater mode is shown in Figure 3-8.

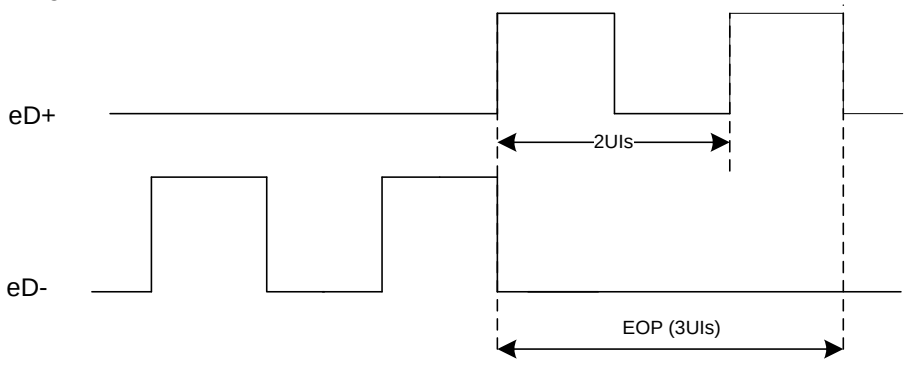


Figure 3-7: Typical Case of FS EOP Pattern

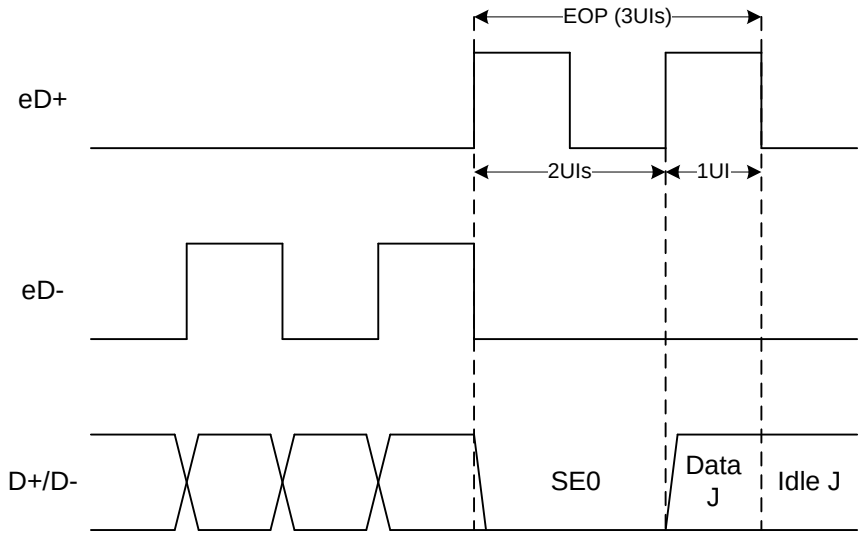


Figure 3-8: Example of eUSB2 EOP to USB2.0 EOP Conversion

- A FS EOP transmitted by an eDSPp or eUSPh is between 1 to 2 UIs of logic ‘1’ at eD+, while eD- is maintained at logic ‘0’. This is shown in Figure 3-9. Similarly, a LS EOP, transmitted by an eDSPp or eUSPh, may be between 1 and 2 UIs of logic ‘1’ at eD-, while eD+ is maintained at logic ‘0’. An eDSPr or eUSPr shall declare the reception of a FS/LS EOP within 3 UIs upon detecting the start of the EOP.

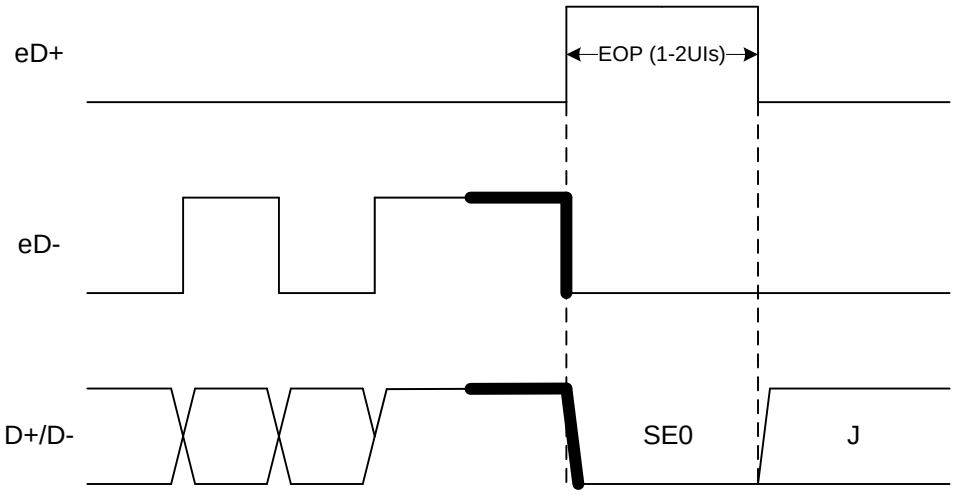


Figure 3-9: EOP Pattern (last J in bold may be a dribble bit if SE0 is only one UI) Full-speed Operation

- eUSB2 high-speed SYNC and EOP patterns are the same as defined by USB2.0, except that the voltage swing is redefined.

3.5 *Control Message Signaling*

Control messages are defined for various USB2.0 and non-USB2 usages in native mode and repeater mode. A control message may be issued by an eDSPn, eDSPr or eUSPr. It either indicates reset, entry to L1/L2, the start of the register access, or disconnect detect enable.

A general example of a control message is shown in Figure 3-10. The encoding and decoding of a control message is defined in Table 3-3 and Table 3-4 based on the number of pulses “n” within the active window (T_{CM_ACTIVE}) defined by the duration of driving logic “1” at eD+. Note that decoding of a control message has a +1 count error tolerance. A port transmitting a control message shall adhere to the following rules:

- It shall wait until the eUSB2 bus state is SE0 before initiating a control message.
- It shall always begin CM transmission with SE1 as Start of Control Message (SCM).
- Following SCM, it shall drive SE0 for $T_{SE0\_DR\_LSFS}$ before maintaining SE0 with R_{PD}.
- It shall monitor the eUSB2 bus state during the SE0 interval. If it has observed SE1, it shall terminate the CM transmission and switch to SE1 detection. Note that the reception of SE1 during SE0 interval implies a contention with ESE1.
- A port receiving the control message shall reset the decoder of the control message upon detecting SCM.

The timing for SE1 and control message signaling varies according to the link state in which the control message is initiated. Refer to Table 6-15 for the timing specification.
A control message is also constructed such that its detection and decoding do not require a clock. A port in L1 or L2 may implement an SE1 detector and use the assertion of the SE1 detector to trigger the control message reception based on a counter that is enabled during the active window set by eD+, and incremented by each pulse received at eD-. At the end of the active window, the count value may be decoded for the control message.

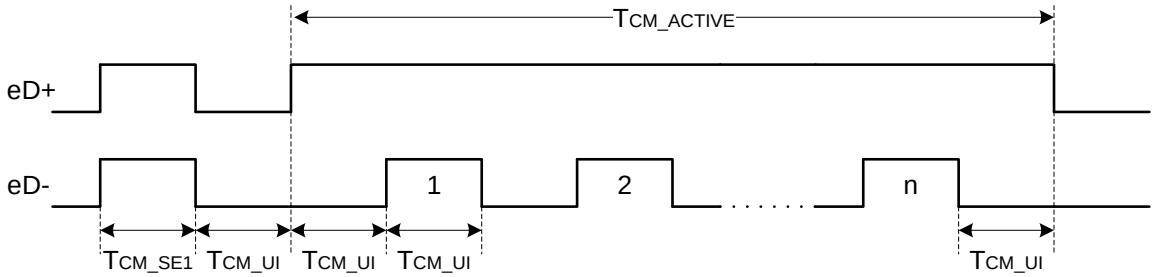


Figure 3-10: eUSB2 Control Message Encoding

Table 3-3: Encoding of eUSB2 Control Message

n	Description	Control Message Name	Usage Cases
0	LineState detect	CM.Zero	Repeater mode only: • In L0 only, for eUSPr directing its peripheral repeater to differentiate between suspend and USB2.0 bus reset in HS operation. Refer to Section 4.2.7.3 for details.
2	L1 entry[2]	CM.L1	Repeater mode only
4	L2 entry	CM.L2	Repeater mode only
6	Disconnect detect enable[3]	CM.Detect	Repeater mode only
8	Default eUSB2 repeater mode	CM.Default	Repeater mode only

10	Host eUSB2 repeater mode	CM.Host	Repeater mode only
12	Peripheral eUSB2 repeater mode	CM.Peripheral	Repeater mode only
15	Reserved		
16	Start of register access[1]	CM.RAP	Native mode: • For eDSPn to access the register space in eUSPn. Repeater mode: • For eUSPr or eDSPr to access the register space in its associated repeater.
20	Reset with default Rx termination scheme[4]	CM.Reset	Both native mode and repeater mode
25	Reset with alternative Rx termination scheme[5]	CM.Reset	Both native mode and repeater mode
>28	Reserved	Reserved	Reserved

Note 1. Indication of the start of register access protocol. Refer to Chapter 5 for details.

Note 2. Entry to L1 for native mode is based on a LPM extended transaction. Use of a control messages to indicate entry to L1 is primarily used for eUSB2 repeaters. Refer to section 4.5 for details.

Note 3. Host repeater shall only enable disconnect detection after entry to L2 and detection of CM.Detect. Refer to Section 2.2.1.10 of [UTMI+ v1.0] for details.

Note 4. In native mode, the default Rx termination scheme is unterminated. In repeater mode, the default Rx termination (R_{RCV_DIF}) scheme is terminated. Please refer to Table 6-3 in Section 6.1.2

Note 5. In native mode, the alternative Rx termination scheme is terminated. In repeater mode, the alternative Rx termination (R_{RCV_DIF}) scheme is unterminated**.** Please refer to Table 6-3 in Section 6.1.2

Table 3-4: Decoding of eUSB2 Control Message

n	Description	Control Message Name
0-1	LineState detect	CM.Zero
2-3	L1 Entry	CM.L1
4-5	L2 Entry	CM.L2
6-7	Disconnect detect enable	CM.Detect
8-9	Default eUSB2 repeater mode	CM.Default
10-11	Host eUSB2 repeater mode	CM.Host
12-13	Peripheral eUSB2 repeater mode	CM.Peripheral
14-15	Reserved	

16-17	Start of register access	CM.RAP
18-22	Reset with default Rx termination scheme	CM.Reset
23-27	Reset with alternative Rx termination scheme	CM.Reset
>28	Reserved	Reserved

3.6 *Disconnect Detect*

The mechanisms of eUSB2 disconnect detect at LS/FS and HS are different from USB2.0 and apply to two operating modes. One is native mode between eUSPn and eDSPn. The other is in repeater mode either between eUSPr and eDSPp, or eUSPh and eDSPr.

3.6.1 Low-speed/Full-speed Disconnect Detect

The SE0 idle state of eUSB2 is maintained by both ports through their R_{PD}. This is different from idle state J defined in [USB2.0] that allows for disconnect detect during idle state. A digital mechanism is defined for eUSB2 device disconnect detect during L0.

- The device disconnect in L0 based on the following defined digital mechanism shall apply in native mode between eDSPn and eUSPn, and the repeater mode between eDSPp and eUSPr. Note that device disconnect detect in repeater mode between eDSPr and eUSPh is achieved based on device disconnect announcement, or repeater presence announcement.

3.6.1.1 Disconnect Detect during L0

A eUSPn or eUSPr in L0 periodically transmits a digital ping to announce its presence. The absence of the digital ping and any packet from a eUSPn or eUSPr is an indication of device disconnect. A digital ping is defined as a digital pulse of variable duration transmitted at eD- or eD+ during EOP reception. An example of the FS digital ping transmission is shown in Figure 3-11.

- A eUSPn or eUSPr shall transmit a digital ping within the window of EOP. It shall transmit the digital ping based on the following:
  - It shall start transmitting the digital ping within T_{PING_LSFS} of detecting the start of EOP based on the rising edge of eD+ for FS or eD- for LS. Note that there may be a short period of contention at eD+/eD- when an eDSPn or eDSPp is still driving eD+/eD- to logic ‘0’ within $T_{SE0\_DR\_LSFS}$ before switching to pull down and an upstream port is driving the digital ping at eD+/eD- upon detection of the start of the EOP.
  - It shall drive the digital ping for 2 UIs.
- A eUSPn or eUSPr shall transmit the digital ping upon detecting the start of EOP.
- An eDSPn or eDSPp in FS operation shall sample at eD- for digital ping during the EOP period.
- An eDSPn or eDSPp in LS operation shall sample at eD+ for digital ping during the EOP period.
- An eDSPn or eDSPp shall declare device disconnect during L0, if both of the following conditions are met:
  - It has not received any packet.
  - It has not received any digital ping within three consecutive EOPs.
- An eDSPn or eDSPp, upon declaring device disconnect, may transmit a DSP reset announcement. Note that the lack of any digital pings and packets from the device may also infer a device failure and, depending on the host behavior, a downstream port may disable this port. Under this scenario, a downstream port may transmit a DSP reset announcement in an attempt to recover the device.

- An eDSPn or eDSPp shall also declare device disconnect when a device disconnect announcement is received.

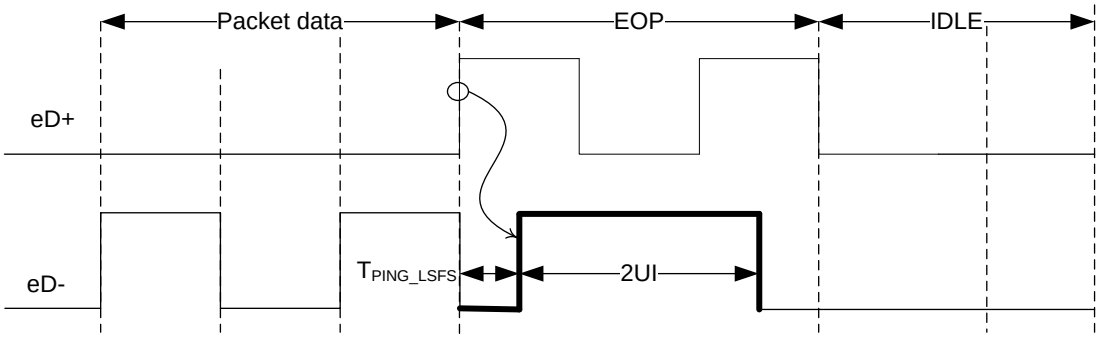


Figure 3-11: FS Digital Ping on EOP

3.6.1.2 Disconnect Detect during L1 and Suspend

A eUSPn or eDSPr performs device disconnect during L1 or L2 based on device disconnect announcement, or USP presence announcement. This also applies to repeater mode between the eDSPp and eUSPr. However, the device disconnect detection based on digital is performed either at the end of resume (LS/FS).

- For LS/FS operation, an eDSPn or eDSPp shall perform disconnect detect during the end of resume by looking for a digital ping.
- For HS operation, an eDSPn or eDSPp shall perform disconnect detection after entry to L0 by looking for an analog ping.
- A eUSPn or eUSPr shall send a digital ping to announce its presence during L1 or L2 at the end of resume. The transmission of digital ping shall follow the requirements defined in Section 3.6.1.1. An example of a FS device announcing its presence at the end of resume is shown in Figure 3-12.
- An eDSPn or eDSPp shall declare the device disconnect if it has not received a digital ping at the end of resume.
- High-speed disconnect detect for an eDSPr is performed based on ESE1 reception.

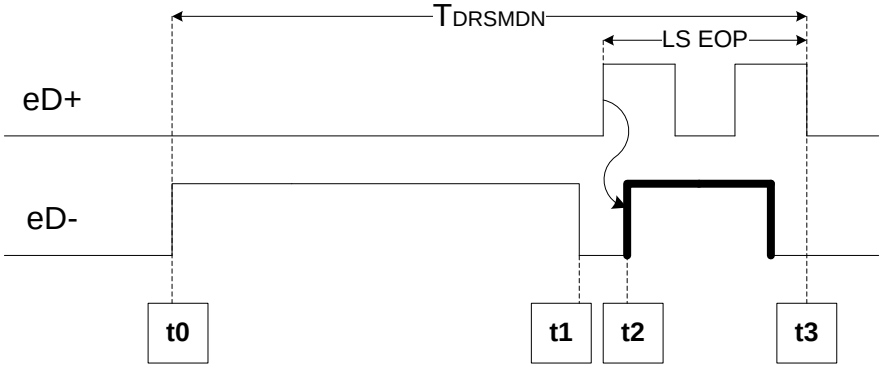


Figure 3-12: Illustration of a eUSPn Transmitting Digital Ping at the End of Resume

t0. eDSPn drives eD- to logic ‘1’ to start resume.
t1. eDSPn transmits LS EOP to conclude resume.
t2. eUSPn, upon detecting the starts LS EOP, transmits a digital ping.
t3. Link enters L0.

3.6.2 High-speed Disconnect Detect

The mechanism for device disconnect detect in HS operation is similar to that in LS/FS operation.

3.6.2.1 High-speed Disconnect Detect during L0

For an eDSPn or eDSPp, high-speed disconnect detect is performed based on eUSPn/eUSPr periodically transmitting an analog ping to the eDSPn/eDSPp to announce its presence. This is illustrated in Figure 3-13. Note also that device or host repeater disconnect detection between an eDSPr and eUSPh is based on device disconnect announcement, or repeater presence announcement (ESE1).

- A eUSPn or eUSPr shall transmit an analog ping within $T_{PING\_D\_HS}$ after detecting the end of HS EOP and no transmit packet is directed. Note that situations exist where, during the analog ping transmission, a transmit packet may be directed or pending. In this case, a eUSPn or eUSPr shall switch from analog ping to packet transmission.
- A analog ping shall be a high-speed data K with pulse width of $T_{PING\_W\_HS}$
- A eUSPn or eUSPr shall enable its squelch detector no later than 6 UIs after the completion of EOP transmission.
- An eDSPn or eDSPp shall declare device disconnect if both of the following conditions are met:
  - It has not received any packets.
  - It has not received any analog pings from the device after the end of HS EOP for three consecutive packets.
- An eDSPr or eDSPp shall declare device disconnect when a device disconnect announcement (ESE1) is received.

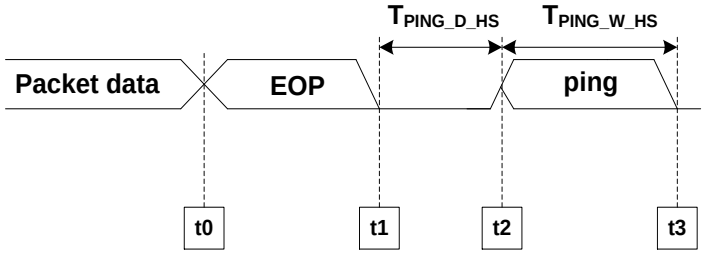


Figure 3-13: Illustration of Device Transmitting an Analog Ping

t0. eDSPr/eDSPp starts transmitting EOP.
t1. eDSPr/eDSPp completes packet transmission.
t2. eUSPn/eUSPr starts transmits the analog ping to announce its presence.
t3. eUSPn/eUSPr completes the analog ping transmission.

3.6.2.2 Disconnect Detect during L1 and Suspend

- An eDSPn or eDSPp shall perform device disconnect in L1 and Suspend based on device disconnect announcement (ESE1) or repeater presence announcement (ESE1).

3.6.2.3 Device Disconnect Announcement

Device disconnect announcement (Section 3.3.1) is an event issued by a eUSPn/eUSPr/eUSPh under one of the following conditions:

- When a eUSPn/eUSPr is directed to terminate its current USB session by disconnecting itself. This is also referred to as graceful device disconnect. The mechanism for triggering device disconnect is implementation specific and out of the scope of this specification.
- When a eUSPh has detected disconnect of a USB2.0 device.
- A eUSPr/eUSPh, upon completing the device disconnect announcement, shall disable its SE transmitters and transition to PVTB.

3.6.2.4 USP Presence Announcement

Compare with device disconnect announcement, which is a graceful event to inform a connected eDSPn/eDSPp about its connectivity. There also exists in scenarios where a eUSPn/eUSPr is disconnected without its associated DSP awareness when the link is L1 or suspend.

- A eUSPn or eUSPr shall initiate USP presence announcement when one of the following scenarios occur:
  - Upon power-up reset.
  - Directed upon HW reset that a new USB session is to be started.
- A eUSPn, upon completing the USP presence announcement, shall proceed to start device connect.
- A eUSPr, upon completing the USP presence announcement, shall proceed to PVTB for TBConfig. Refer to Section 4.2.3 for details.

3.6.2.5 DSP Reset Announcement

Situations may exist where an eDSPn or eDSPr is under global reset, and a device is still connected. Under this situation, a device may enter suspend or L1 with link state maintained as SE0. Upon completion of the global reset, an eDSPn or eDSPr may not be aware of the device connectivity, primarily due to the fact that the eUSB2 idle state is SE0. To address this specific situation, an eDSPn, eDSPr or eDSPp shall adhere to the following rules:

- An eDSPn or eDSPr shall initiate the DSP reset announcement if a new USB session is to be started. This may be due to, but is not limited to, the following conditions:
  - Power-up reset.
  - Loss of connectivity after HW reset.
- Upon completing the DSP reset announcement, an eDSPn shall enable its R_{PD} at eD+/eD- in preparation of USP presence announcement or device connect.
- Upon completing the DSP reset announcement, an eDSPr shall enable its R_{PD} at eD+/eD- and transition to PVTB.
- A eUSPn in L1 or suspend, upon detecting DSP reset announcement, shall terminate the current USB session and initiate connect to start a new USB session.
- A eUSPr/eUSPh, upon detecting DSP reset announcement, shall terminate the current USB session and transition to PVTB.

3.6.2.6 Repeater Presence Announcement

Repeater presence announcement applies to a repeater during initialization before its role as either a host repeater or peripheral repeater is configured.

- A repeater, if directed or upon power-up reset, shall transmit repeater presence announcement and transition to PVTB.

3.7 *PHY State Transition and Power Management*

A conceptual eUSB2 PHY state machine is shown in Figure 3-14. It summarizes the basic behavior of the eUSB2 operation during power-up, connect & resume, which will be described in detail in this section.

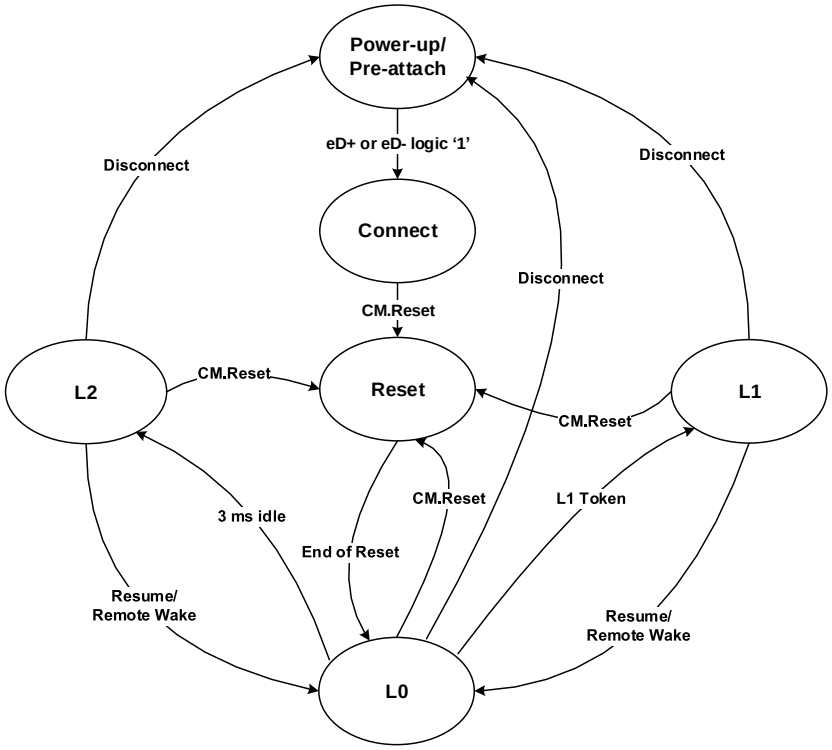


Figure 3-14: eUSB2 PHY State Machine.

3.7.1 Power-up, Connect, and Reset

The power-up sequence may be asynchronous between a downstream port and an upstream port. The outlined time-domain process for link power-up, connect detect, and reset follows [USB2.0]. The mechanism for connect detection is different. The port shall perform the following from connect detect upon power-up to end of device reset:

- Upon power-up the port shall perform the following:
  - An eDSPn, eDSPr or eDSPp shall perform the following:
    - It shall enable its R_{PD} at eD+ and eD-.
    - It shall transmit a DSP reset announcement (ESE1) as defined in Section 3.3.1 before disabling its transmitters.
    - Upon completing DSP reset announcement, it shall enable its SE receivers and wait for USP presence announcement or device connect. Note that a eUSB2 device may power up first and have completed the USP presence announcement.
  - An eUSPn, eUSPh or eUSPr shall enable its R_{PD} and single-ended receiver at either eD+ or eD- based on the following:
    - It shall enable its R_{PD} at eD+ and eD-.
    - It shall transmit the USP presence announcement as defined in Section 3.3.1.
- Upon direction after completing the USP presence announcement transmission or detecting the DSP reset announcement, an eUSPn, eUSPh or eUSPr shall signal connect based on the following:
  - If it operates at full-speed/high-speed, and observes logic '0' at eD-, it shall drive logic '1' at eD+. Note that if it observes logic '1' at eD-, it may indicate a downstream port is transmitting a CM.RAP or DSP reset announcement and shall wait until eD- is logic '0', then initiate connect.

    - If it operates at low-speed and observes logic ‘0’ at eD+, it shall drive logic ‘1’ at eD-. Note that if it observes logic ‘1’ at eD+, it shall wait until eD+ is logic ‘0’, then initiate connect.
    - Upon driving logic ‘1’ at eD+ (FS/HS) or eD- (LS) to signal connect and observing logic ‘1’ at eD- (FS/HS) or eD+ (LS) at the same time, it shall disable its transmitter to terminate connect and examine if SE1 is detected. If it is ESE1, it shall wait until the completion of ESE1 before signaling device connect again; if it is SCM, it shall prepare for CM.RAP reception. Note that this is a concurrent situation where a downstream port is transmitting CM.RAP or DSP reset announcement at the same time an upstream port is signaling connect. An upstream port shall uphold connect and complete the CM.RAP or DSP reset announcement reception before resuming connect.
- Upon detecting USP presence announcement, an eDSPn, eDSPr or eDSPp shall proceed for device connect detection. Note that a downstream port may or may not receive USP presence announcement depending on the power-up sequence.
- Upon detecting device connect, an eDSPn, eDSPr or eDSPp shall perform debounce for the period as defined by [USB2.0]. A downstream port shall declare device connect and acknowledge the device accordingly based on one of the following:
    - If it has detected logic ‘1’ at eD+ and logic ‘0’ at eD- for T_{ATTDB} duration, it shall start driving logic ‘1’ at eD- for T_{ACK}.
    - If it has detected logic ‘0’ at eD+, and logic ‘1’ at eD- for T_{ATTDB} duration, it shall start driving logic ‘1’ at eD+ for T_{ACK}.
- Upon detecting acknowledgement from the eDSPn/eDSPr/eDSPp, a eUSPn/eUSPh/eUSPr shall do the following:
    - If it operates at full-speed/high-speed it shall:
        - Drive logic ‘0’ at eD+ for $T_{SE0\_DR\_LSFS}$ and then disable its eD+ transmitter.
        - Enable its single-ended receiver at eD+.
    - If it operates at low-speed it shall:
        - Drive logic ‘0’ at eD- within $T_{SE0\_DR\_LSFS}$ and disable its transmitter.
        - Enable its single-ended receiver at eD-.
- An eDSPn, eDSPr or eDSPp shall complete the acknowledgement and declare the following:
    - If it is driving eD- for acknowledgement, and observes logic ‘0’ at eD+ at the end of T_{ACK}, it shall declare full-speed/high-speed device connect. Note that if logic ’1’ at eD+ is observed at the end of acknowledgement, it implies that a dual role repeater is reporting the de-assertion of PeripheralEnb. Refer to Section 4.2.7.6 for details.
    - If it is driving eD+ for acknowledgement, and observes logic ‘0’ at eD- at the end of T_{ACK}, it shall declare low-speed device connect. Note that if logic ’1’ at eD- is observed at the end of acknowledgement, it implies that a dual role repeater is reporting the assertion of HostEnb. Refer to Section 4.2.7.6 for details.
- A eUSPn shall enter suspend if it has detected idle state for the duration of 3ms.
- Upon directed by the host controller, an eDSPn, eDSPr or eDSPp shall issue CM.Reset to initiate device reset.
- A eUSPn, eUSPh or eUSPr shall enter reset upon detection of CM.Reset. A high-speed capable upstream port shall perform the additional CM.Reset decoding for receiver termination scheme. Refer to Section 3.5 for details.
- An eDSPn, eDSPr or eDSPp shall perform the speed detection as defined in [USB2.0]. Refer to Section 3.7.3 for eUSB2 specific speed detection signaling.
- An eDSPn, eDSPr or eDSPp shall perform one of the following to conclude reset:
    - If it operates at LS, it shall transmit a LS EOP to conclude reset.
    - If it operates at FS, it shall transmit a FS EOP to conclude reset.

- If it operates at HS, it shall transmit a single acknowledgement pulse at eD+ at the end of host chirp acknowledgement to conclude reset. Refer to section 3.7.3 for definition of high-speed end of reset.

- An eDSPn, eDSPr or eDSPp shall conclude reset by driving SE0 and enter reset recovery with SE0 maintained through its R_{PD}.
- A eUSPn, eUSPh or eUSPr, upon detecting end of reset, shall be in the default state defined by [USB2.0].

Shown in Figure 3-15 is the interactions between the two eUSB2 ports operating at FS.

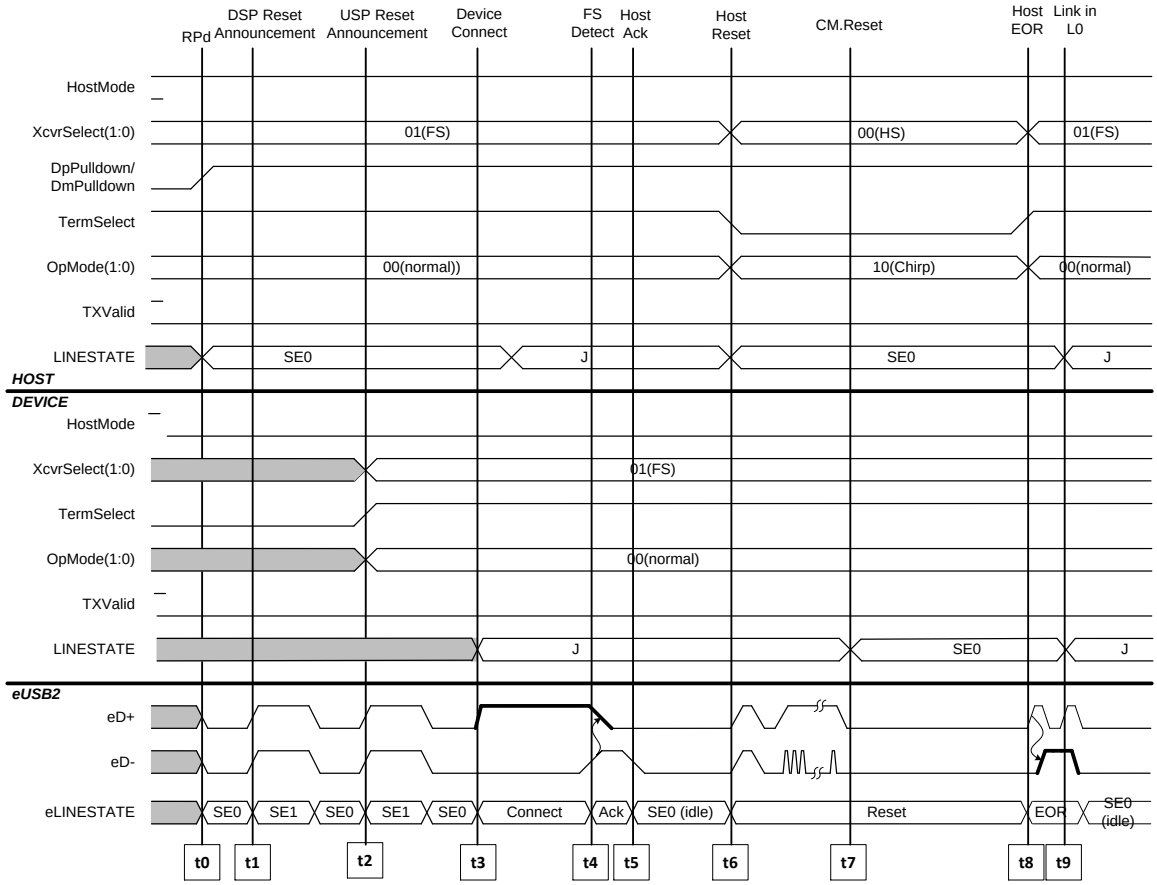


Figure 3-15: Time-domain Illustration of Power-up and Device Detect. A Full-speed Device is used as an Example (Native Mode)

t0. An eDSPn, upon power-up, enables its R_{PD} at eD+/eD-. The link is SE0.
t1. An eDSPn, transmits a DSP reset announcement.
t2. A full-speed capable eUSPn, upon power-up, enables its R_{PD}, and transmits an USP presence announcement.
t3. A eUSPn signals connect by driving logic ‘1’ at eD+.
t4. After completion of debouncing, an eDSPn drives an acknowledgement at eD- to acknowledge device connect. A eUSPn, upon detecting the acknowledgement at eD-, drives eD+ to logic ‘0’ and disable its SE transmitter at eD+.
t5. An eDSPn concludes connect acknowledgement.
t6. An eDSPn transmits CM.Reset to initiate start of reset.
t7. A eUSPn, upon detecting CM.Reset, enters reset.
t8. An eDSPn concludes reset by transmitting a FS EOP. A eUSPn or eUSPr, upon detecting start of EOP, transmit a digital ping to indicate its presence.

t9. An eDSPn or eDSPp, upon concluding the EOP transmission, and reception of the digital ping, enters L0. An eDSPr upon concluding the EOP transmission enters L0. A eUSPn or eUSPr, upon transmitting the digital ping, and reception of EOP, enters L0. A eUSPh upon reception of EOP, enters L0.

3.7.2 Suspend, Resume and Remote Wake

The policies for suspend, resume, and remote wake are similar to USB2.0 except that the entry to Suspend is explicitly based on control message.

3.7.2.1 Suspend and Resume

For entry to suspend, the port shall adhere to the following rules:

- A downstream port shall transition to suspend when directed. An eDSPr shall transmit a CM.L2 before entering suspend.
- An upstream port shall enter suspend if it has detected link idle for the duration of 3ms. A eUSPh shall enter suspend after reception of a CM.L2.

For resume from suspend, the port shall adhere to the following rules:

- A downstream port shall initiate resume by transmitting the resume signal defined below with timing defined in [USB2.0].
  - If operating at full-speed/high-speed, it shall drive the resume signal at eD-.
  - If operating at low-speed, it shall drive the resume signal at eD+.

  Note: The use of eD- to resume from full-speed/high-speed operations, and eD+ to resume from low-speed operation, is to avoid potential contention if a eUSB2 device is disconnected during suspend and starts connect at the same time a downstream port initiates exit from resume.
- A downstream port shall conclude resume by performing on of the following:
  - If operating at full-speed, it shall transmit a LS EOP at eD+. An eDSPn or eDSPp shall also perform device presence detect during EOP transmission.
  - If operating at low-speed, it shall transmit a LS EOP at eD-. An eDSPn or eDSPp shall also perform device presence detect during EOP transmission.
  - If operating at high-speed, it shall transmit an end of resume signal at eD+. The end of resume signal shall be the same as the digital ping with 2 UIs of LS duration.
- Upon detecting the resume signal, an upstream port shall proceed to exit from suspend based on the following:
  - A eUSPn or eUSPr operating at full-speed, shall transmit a digital ping at eD- upon detecting the LS EOP at eD+ and enter L0.
  - A eUSPh operating at full-speed, upon detecting the LS EOP at eD+, shall enter L0.
  - A eUSPn or eUSPr operating at low-speed, shall transmit a digital ping at eD+ upon detecting the LS EOP at eD- and enter L0.
  - A eUSPh operating at low-speed, upon detecting the LS EOP at eD-, shall enter L0.
  - If it is operating at high-speed, it shall enter L0 upon detecting the end of resume.
- An eDSPn or eDSPp shall enter connect if it has not received the digital ping at the end of resume.

Shown in Figure 3-16 and Figure 3-17 are example timing diagrams of suspend entry and resume for low-speed/full-speed operation.

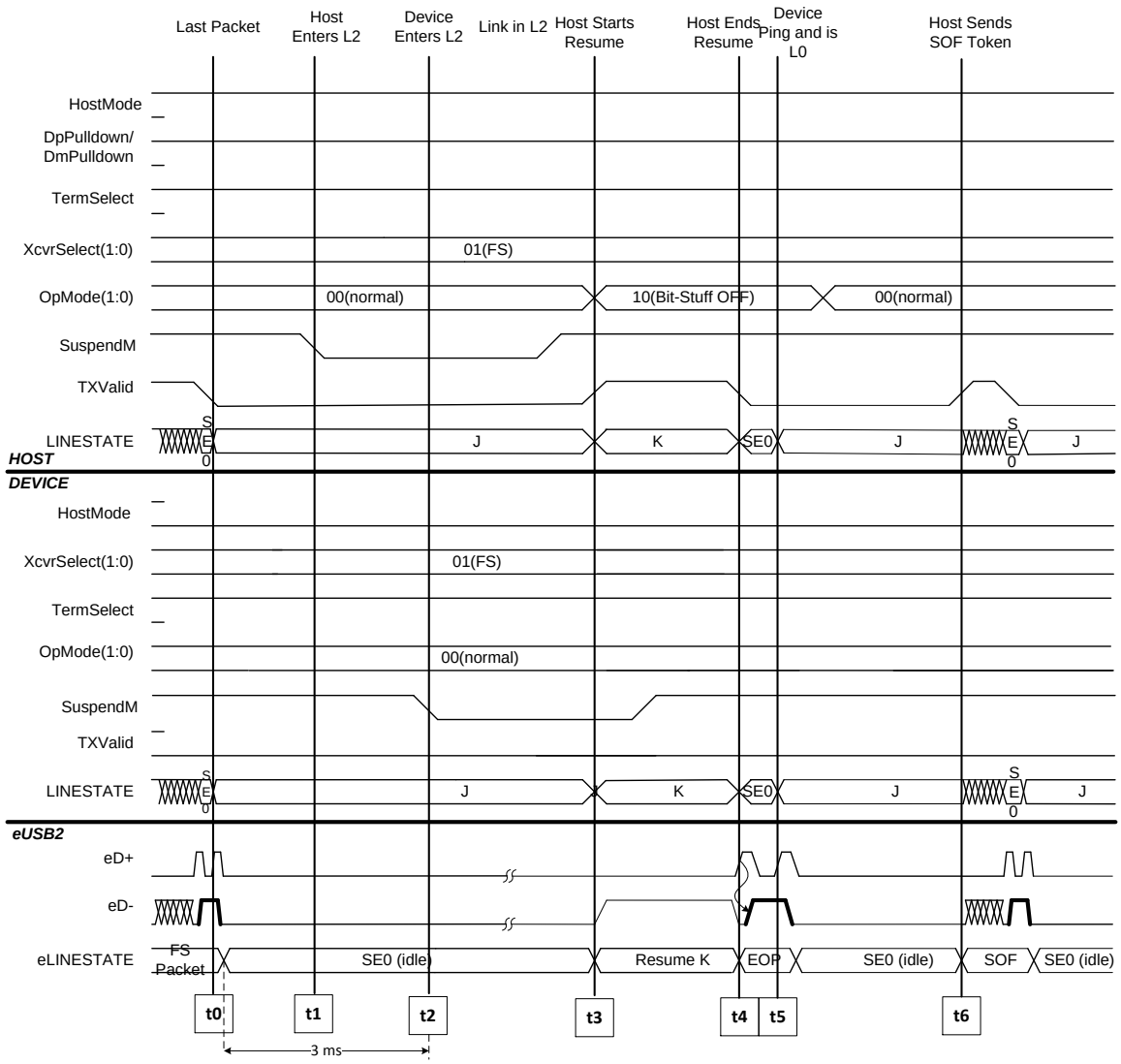


Figure 3-16: Full-speed Suspend and Resume for native eUSB2 (Native Mode)

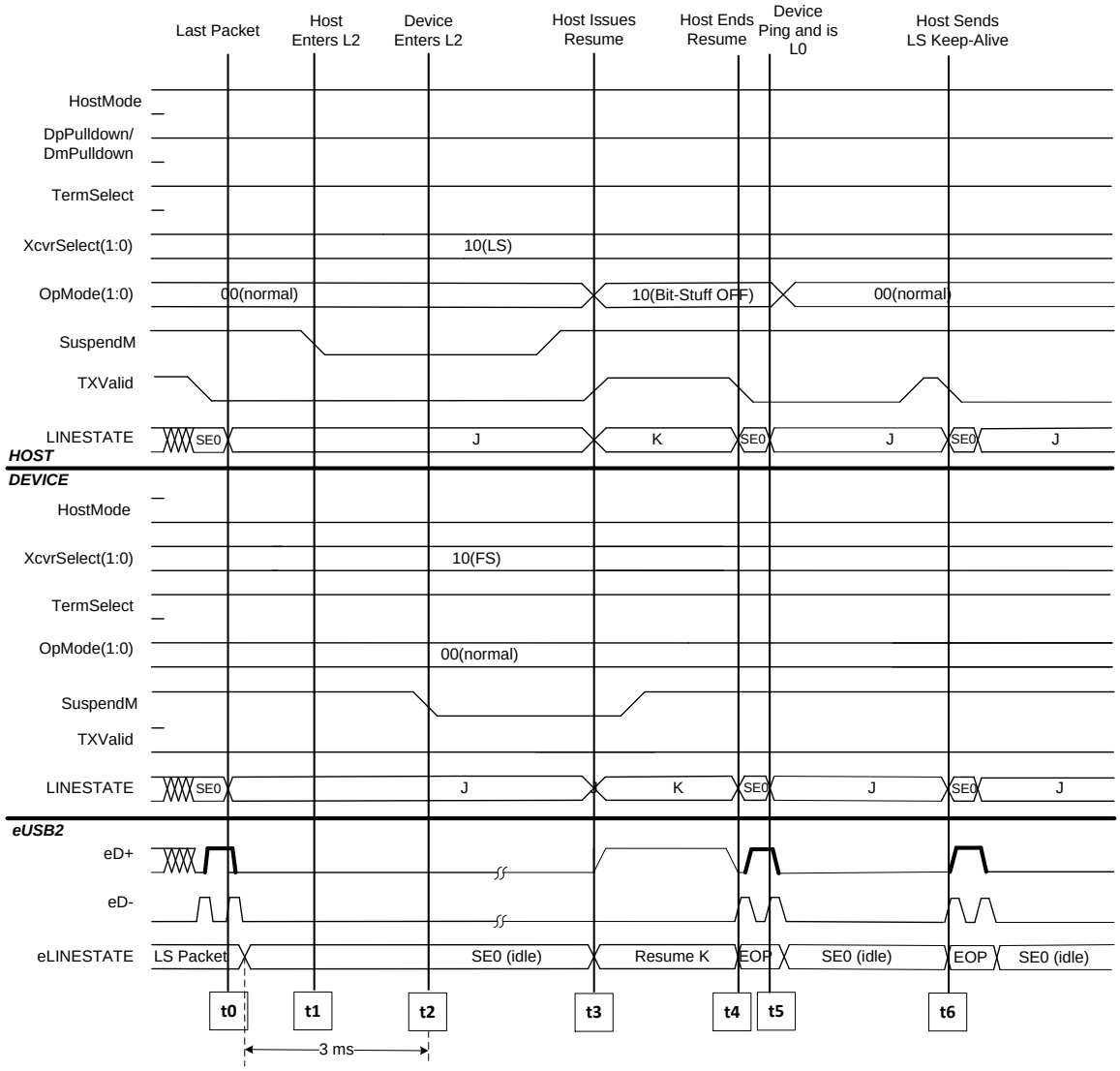


Figure 3-17: Low-speed Suspend and Resume for native eUSB2 (Native Mode)

t0. Link enters idle.
t1. An eDSPn transitions to suspend when directed. An eDSPr shall transmit a CM.L2 before entering suspend.
t2. A eUSPn transitions to suspend upon 3ms link idle. Note that for implementation based on UTMI+, a port in high-speed operation may change its linestate from SE0 to J for compatibility to UTMI+ specification.
t3. An eDSPn starts resume. A eUSPn, upon detecting the resume signal, prepares exit from suspend with timing meeting specification defined by [USB2.0] specification.
t4. An eDSPn transmits a LS EOP in LS/FS operation to conclude resume. A eUSPn or eUSPr, if in LS/FS operation, upon detecting the start of LS EOP, transmits a digital ping to indicate its presence during suspend.
t5. The port concludes resume. Link enters L0 idle.
t6. An eDSPn transmits a SOF (FS) or LS keep-alive (LS) to prevent the device from entering suspend.

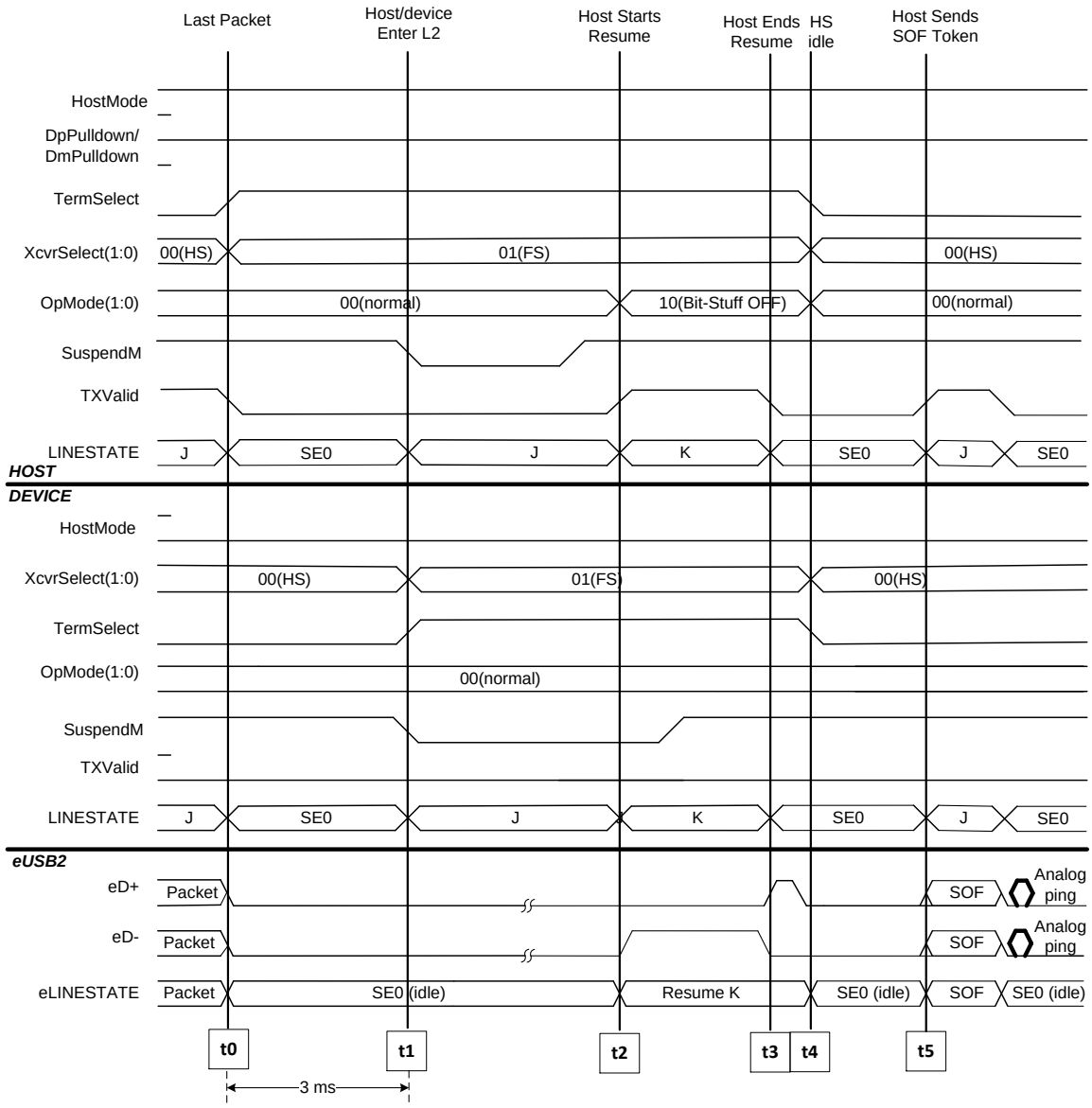


Figure 3-18: High-speed Suspend and Resume Link enters idle (Native Mode)

t0. An eDSPn transitions to suspend when directed. An eDSPr shall transmit a CM.L2 before entering suspend.
t1. A eUSPn transitions to suspend upon 3ms link idle. Note that for implementation based on UTMI+, a port in high-speed operation may change its linestate from SE0 to J for compatibility to UTMI+ specification.
t2. An eDSPn starts resume. A eUSPn, upon detecting the resume signal, prepares exit from suspend with timing meeting specification defined by [USB 2.0] specification.
t3. An eDSPn transmits an acknowledgement if in HS operation to conclude resume. A eUSPn if in HS operation, concludes resume upon detecting the host acknowledgement.
t4. The port concludes resume. Link enters L0 idle.
t5. An eDSPn transmits a SOF to prevent the device from entering suspend.

3.7.2.2 Remote Wake from Suspend

For remote wake from suspend, the port shall adhere to the following rules:

- An upstream port shall initiate remote wake based on the following:
  - If it is operating at full-speed/high-speed, it shall use eD+ to initiate remote wake, the timing of which shall follow [USB2.0].
  - If it is operating at low-speed, it shall use eD- to initiate remote wake, the timing of which shall follow [USB2.0].
- A downstream port, upon detecting remote wake, shall acknowledge resume within T_{URSM} as defined by the [USB2.0]. A downstream port shall perform one of the following:
  - If it is full-speed/high-speed operation, it shall drive the resume signal at eD-, the timing of which shall follow [USB2.0].
  - If it is low-speed operation, it shall drive the resume signal at eD+, the timing of which shall follow [USB2.0].
  - The downstream port shall complete resume as defined in Section 3.7.2.1.

Shown in Figure 3-19 is an example timing diagram of a link in FS operating from entry to suspend, to an upstream port initiating remote wake, and a downstream port following up with resume.

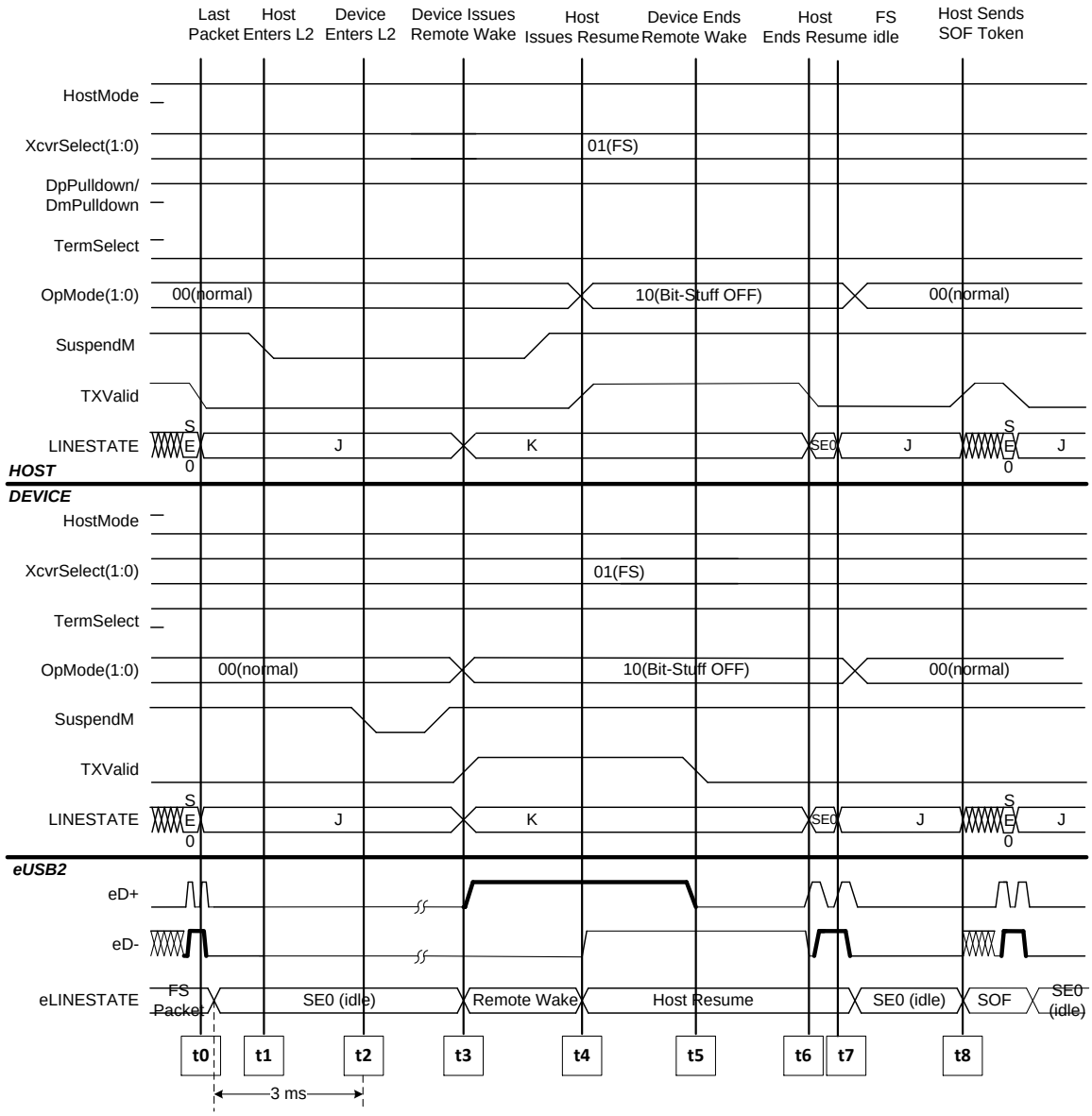


Figure 3-19: FS Suspend and Remote Wake (Native Mode)

t0. Link enters idle.
t1. An eDSPn transitions to suspend when directed. An eDSPr shall transmit a CM.L2 before entering suspend
t2. A eUSPn transitions to suspend upon detecting 3ms link idle.
t3. A eUSPn initiates remote wake at eD+.
t4. An eDSPn drives the resume signal at eD- within period of T_{URSM}.
t5. A eUSPn concludes the remote wake within period of T_{DRSMUP}.
t6. An eDSPn drives eD- to logic ‘0’ and concludes by driving a low-speed EOP at eD+. A eUSPn transmits a digital ping upon detecting the start of EOP.
t7. The port concludes resume. Link enters L0.
t8. An eDSPn starts USB traffic.

3.7.3 High-speed Detection

High-speed detection applies to high-speed operation only and is accomplished using single-ended signaling. The high-speed detection shall adhere to the following rules:

- An upstream port, upon detecting CM.Reset, shall further decode CM.Reset to determine its receiver termination scheme. an upstream port shall determine its receiver termination embedded in CM.Reset based on the following:
  - If the count of CM.Reset is within the range of 16 to 23, as defined in Table 3-4, it shall maintain its default high-speed receiver termination.
  - If the count of CM.Reset is within the range of 24 to 31, as defined in Table 3-4, it shall alternate its high-speed receiver termination from its default setting.
- After entry to reset, an upstream port shall start driving logic ‘1’ at eD- to present it as a device chirp. The duration of this device chirp shall follow the timing defined by [USB2.0] (T_{UCHEND}). Note that the high-speed transmitter and receiver at both ports shall be disabled during reset.
- An upstream port shall conclude device chirp and enable its single-ended receivers at both eD+ and eD- in expectation of host chirp acknowledgment.
- A downstream port, after reception of device chirp, shall drive the host chirp at eD-, the timing of which shall follow [USB2.0].
- An upstream port shall transmit a digital ping to indicate its readiness for high-speed operation. Refer to Section 4.5 for use of this digital ping in peripheral repeater operation. A downstream port may ignore this digital ping.
- A downstream port shall conclude host chirp acknowledgement by driving an acknowledgement signal at eD+ to signal the completion of high-speed detection and reset. The format of the acknowledgement signal shall be the same as the digital ping.
- An upstream port, upon detecting the acknowledgement at eD+, shall enter L0 by enabling its high-speed transceiver.

The example timing diagram of the high-speed detection is described in Figure 3-20.

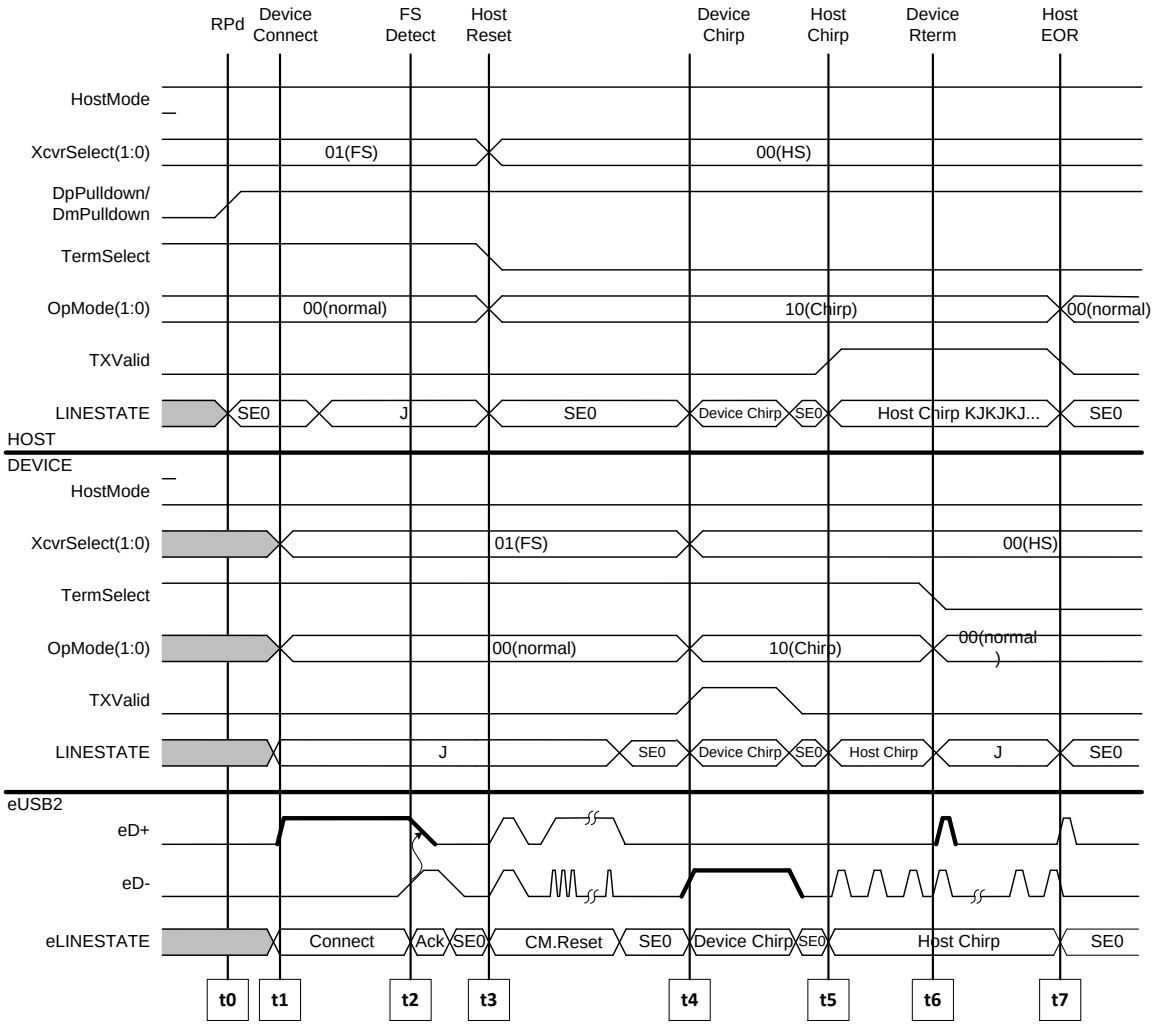


Figure 3-20: Timing Diagram for High-speed Speed Negotiation (Native Mode)

3.7.4 L1 Entry and Exit

eUSB2 shall support LPM-L1 (L1) based on USB2.0 Link Power Management Addendum. The L1 entry is initiated through L1 extended transaction as described in USB2.0 Link Power Management Addendum.

- Upon receiving L1 acknowledgement from the eUSB2 device, an eDSPn or eDSPr shall transition to L1.
- Upon sending the L1 acknowledgment, a eUSPn or eUSPr shall prepare L1 entry no earlier than $T_{L1TokenRetry}$ (min), and no later than $T_{L1TokenRetry}$ (max) as defined by the ECN for USB2.0 Link Power Management Addendum. It shall be in L1 within the minimum L1 residency time defined by the addendum.
- The behaviors of L1 exit shall be the same as L2 exit.
- The timing of L1 entry and exit shall follow the ECN for USB2.0 Link Power Management Addendum.
- If a native eUSB2 port (upstream or downstream) is connected to a eUSB2 repeater, it will transmit a CM.L1 before transitioning to L1.

Shown in Figure 3-21 and Figure 3-22 are example timing diagrams of port entering L1 and exit from L1 based on host resume or device remote wake.

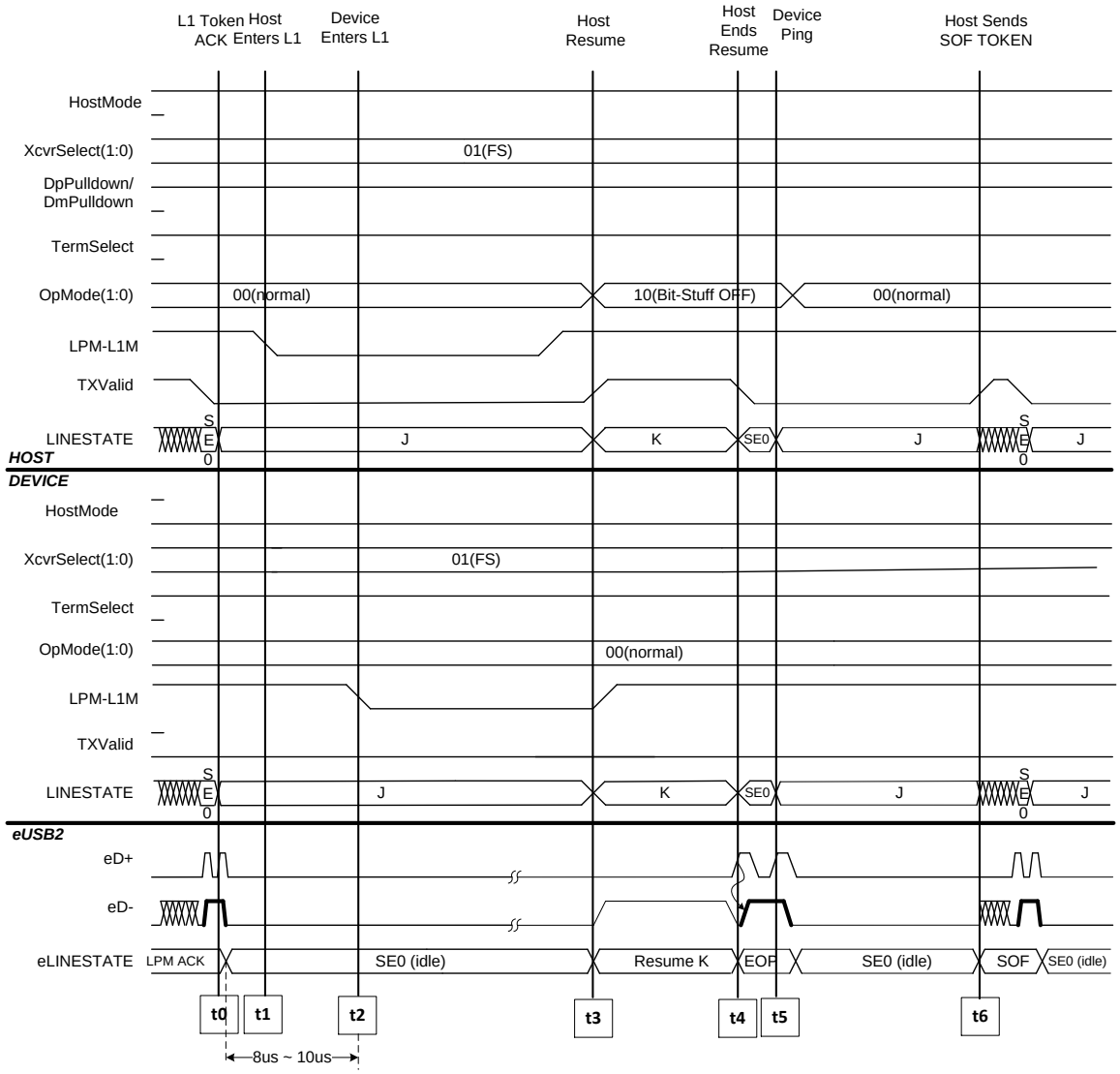


Figure 3-21: FS L1 Entry and Resume (Native Mode)

t0. A eUSPn completes the LPM token acknowledgement.
t1. An eDSPn transitions to L1 when directed. An eDSPr shall transmit a CM.L1 before entering L1.
t2. A eUSPn or eUSPr prepares transition to L1 upon link idle for at least $T_{L1TokenRetry}$ (min) and no later than $T_{L1TokenRetry}$ (max). An eDSPp and a eUSPh transition to L1 upon reception of CM.L1.
t3. An eDSPn starts resume by driving logic ‘1’ at eD-.
t4. An eDSPn concludes resume by driving a low-speed EOP. A eUSPn or eUSPr, upon detecting the start of EOP, transmits a digital ping to indicate its presence.
t5. The port concludes resume and enters L0.
t6. An eDSPn starts the USB traffic.

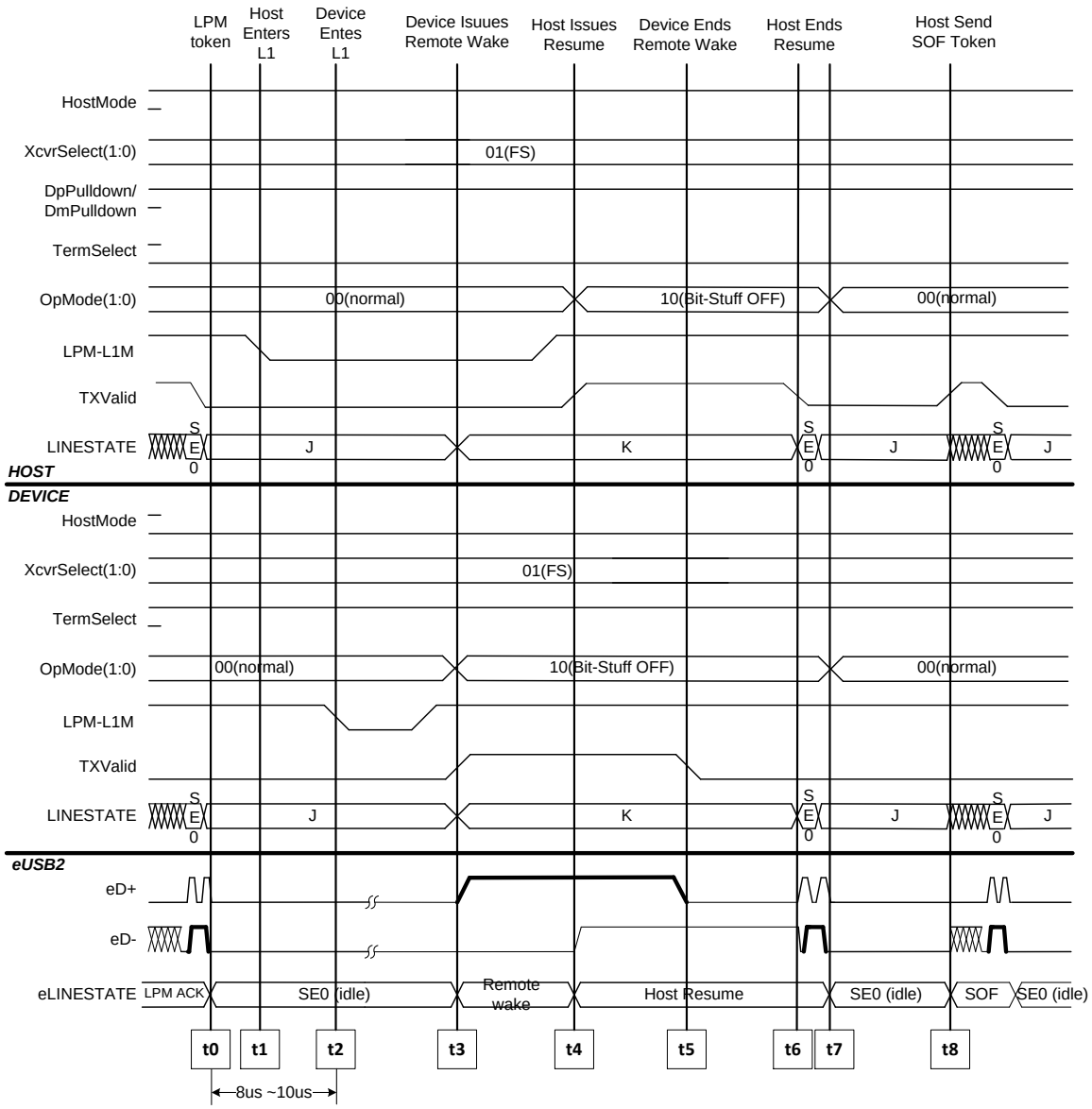


Figure 3-22: FS L1 Entry and Remote Wake (Native Mode)

t0. A eUSPn completes the LPM token acknowledgement.
t1. An eDSPn transitions to L1 when directed. An eDSPr shall transmit a CM.L1 before entering L1.
t2. A eUSPn and a eUSPr prepares transition to L1 upon link idle for at least $T_{L1TokenRetry}$ (min) and no later than $T_{L1TokenRetry}$ (max). A eUSPr shall transmit a CM.L1 before entering L1. An eDSPp and a eUSPh transition to L1 upon reception of CM.
t3. A eUSPn initiates remote wake at eD+. (Note that full-speed is used as an example).
t4. An eDSPn starts resume at eD-.
t5. A eUSPn ends the remote wake signal.
t6. An eDSPn drives eD- to logic ‘0’ and then concludes resume by driving a LS EOP. A eUSPn or eUSPr, upon detecting the start of EOP, transmits a digital ping.
t7. The port concludes remote wake and resume and enters L0.
t8. An eDSPn starts the USB traffic.

3.7.5 Disconnect and Reconnect in L1 or Suspend

In the event of a device disconnecting itself and initiating connect during suspend, or less likely L1, a downstream port shall announce the device disconnect followed by device connect based on the following rules.

- Upon detection of device connect, a downstream port shall declare device disconnect within T_{DDIS} defined by [USB2.0].
- A downstream port shall declare device connect within T_{CONN} after signaling device disconnect.

3.7.6 Reset during L0, L1 or Suspend

An upstream port in L0, L1, or L2 shall enter reset if it has detected CM.Reset as defined in section 3.5. Refer to Section 3.7.1 and Section 3.7.3 for behaviors of an upstream port during reset.

3.8 *Low-speed Keep Alive Signaling*

Low-speed keep alive is a specific case where an EOP is transmitted by the downstream port to prevent a peripheral device from entering suspend. The low-speed keep alive signaling is the same as the LS EOP.

3.9 *Speed Configuration*

Native mode eUSB2 operation is defined to support in-box interconnect where the speed of the eUSB2 operation maybe preconfigured. This usage model may allow an opportunity for a downstream port to support only a single or selected speed configurations, and hence, implementation optimization may be possible based on port customization. However, it is a system's responsibility to be aware of a downstream port's capability and to ensure proper device configuration and interoperability.

- A customized downstream port supporting a single or selected data rates shall follow the eUSB2 specification as defined in Section 3.7.1 in terms of device connect, reset and speed detection. Note that a downstream port that supports high-speed only operation is still required to perform speed detection protocol, even it knows a priori that a device attached is high-speed capable.

Examples of downstream port configurations include but are not limited to the following:

- LS, FS, HS
- LS, FS only
- FS, HS only
- FS only
- HS only

4 eUSB2 Repeater Architecture and Operation

Focusing on implementation simplicity with the lowest power consumption and cost addition, this chapter describes the architecture and operation of a eUSB2 Repeater compliant to [USB2.0] specification.

4.1 *eUSB2 Repeater*

A eUSB2 Repeater is working with a eUSB2 PHY in SOCs to support:

- USB2 host root hub DSP (Host Repeater)
- USB2 peripheral USP (Peripheral Repeater)
- USB2 DRD port (DRD Repeater)

4.1.1 Scope of Specification

In this specification, distinctions are made between:

- eUSB2 Repeater Core: A functional block introduced by eUSB2. Its architecture and operations are specified in this section. In this chapter, unless otherwise specified, the term of “repeater” refers to “repeater core”.
- eUSB2 Repeater Implementation: vendor specific, it includes the Repeater Core as specified and optionally other system components, such as DRD Role Logic, Host/Peripheral V_{BUS} qualification, V_{BUS} Power Switch, Battery Charging, etc.

Note that all optional components of a eUSB2 Repeater implementation are out of scope of eUSB2 specification. For instance,

- DRD Role Logic: specified by [USB2 OTG].
- Battery Charging: dictated by [BC1.2].
- Host Power Switch: described in [USB2.0].

In addition, eUSB2’s interfaces to a USB controller and that to optional system component (such as Battery Charging and USB Power Switch) are also considered vendor specific and therefore out of scope of this specification.

4.1.2 Session Controller (SC)

The Session Controller (SC) is responsible for initiating and terminating a USB session and enables and disables the Repeater Core. The SC works in conjunction with the USB controller and its eUSB2 PHY. It may be implemented in the repeater or in the SoC. As a minimum,

- SC for a USB Host (SCH) shall include V_{BUS} Supplying circuits (V_{BUS} Power Switch and Over Current Detection).
- SC for a USB Peripheral (SCP) must support V_{BUS} Qualification (for example, Level shifting and De-bouncing).
- SC for a USB DRD (SCD) shall contain DRD Role Logic as well as circuits for SCH and SCP.

It is assumed by this specification at the time when a USB session is ready to be launched, a:

- Output HostEnb is asserted by the SCH for a USB Host.
- Output PeripheralEnb is asserted by the SCP for a USB Peripheral.
- Output HostEnb or PeripheralEnb (but not both) is asserted by the SCD according to the outcome of its DRD Role Logic.

A SC implementation:

- May involve a set of control/status signals from/to the SOC that includes a USB Controller.
- May support Battery Charging, full OTG protocols, etc. in addition to the minimum requirements stated above.
- Is vendor specific in nature, and therefore out of the scope of this specification.

Note that the concept of the SC is applicable to any USB Controller, not just for [USB2.0] or eUSB2. It is introduced in this spec to decouple the functionality of the SC and that of eUSB2 Repeater Core.

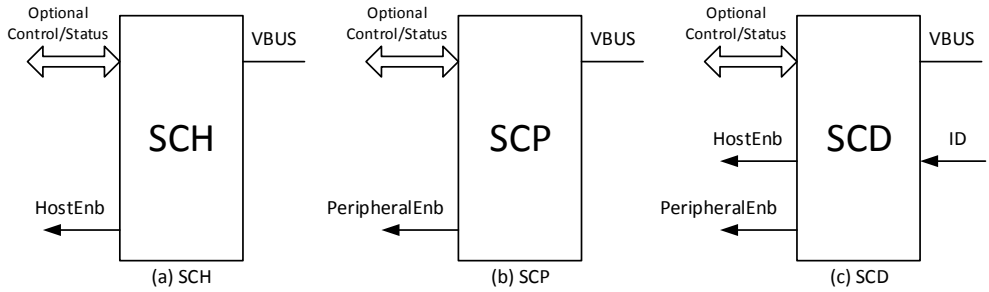


Figure 4-1: SC for Host, Peripheral and DRD

4.1.3 Top Down/Bottom Up Configuration

A eUSB2 Repeater must be configured for Top Down or Bottom Up operation before a USB session can be initiated by the SC. Top Down or Bottom Up configuration (TBConfig) can be determined during the verification of eUSB2 Repeater presence detection upon power up. Refer to Section 4.2.5 for details. Note that the choice of which configuration to support is implementation specific based on system requirements.

- Top Down (TD), where the launching of a USB Session (HostEnb/PeripheralEnb) is

- Originated by a SC and passed to the USB Controller in SOC
- Relayed by a USB Controller to its eUSB2 PHY
- Commanded by eUSB2 PHY to eUSB2 Repeater

- Bottom Up (BU), where the launching of a USB Session (HostEnb/PeripheralEnb) is

- Originated by a SC and passed to a eUSB2 Repeater
- Announced by the eUSB2 Repeater to its eUSB2 PHY in SOC
- Indicated by eUSB2 PHY to the USB Controller

A eUSB2 Repeater must be configured to work under Top Down or Bottom Up before a USB session can be launched.
TBConfig can be determined during the required verification of eUSB2/Repeater presence upon power on. Refer to Section 4.2.5 for details.

4.1.4 Architecture and Interface

The architecture of a eUSB2 repeater core is a half-duplex non-linear redriver. A simplified eUSB2 repeater block diagram is shown in Figure 4-2.

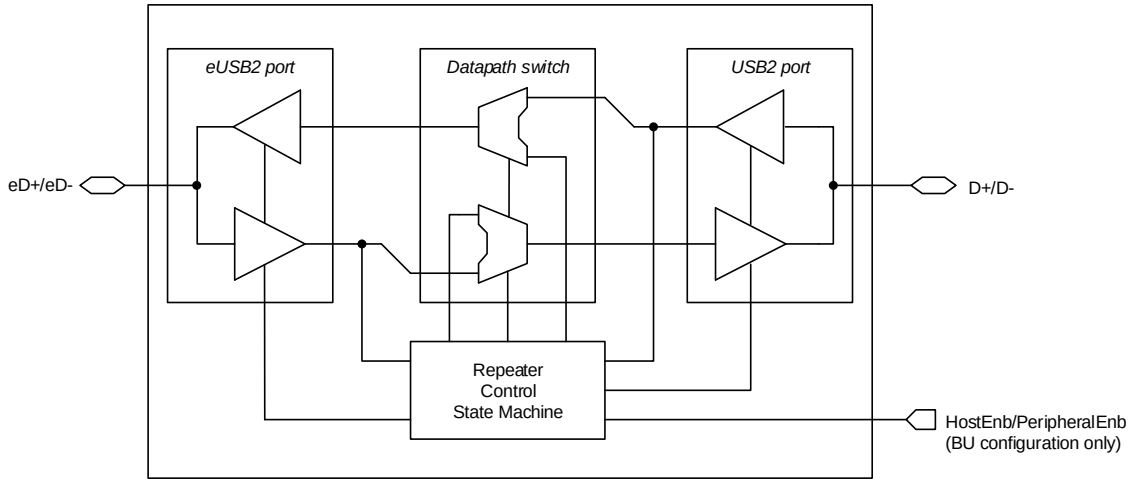


Figure 4-2: eUSB2 Based Repeater Core Architecture

Interfacing signals of a Repeater core is listed in Table 4-1.

Table 4-1: Repeater Core IO Description

	Direction	Description
eD+/eD-	Input/Output	data pins of the eUSB2 port
D+/D-	Input/Output	data pins of the USB2.0 port
HostEnb	Input	Used only for Host and DRD Repeater in Bottom Up configuration. Asserted by the SC after it has determined that the local Repeater/eUSB2/Controller may now be enabled for Host mode operation. HostEnb and PeripheralEnb are mutually exclusive.
PeripheralEnb	Input	Used only for Peripheral and DRD Repeater in Bottom Up mode. Asserted by the SC after it has determined that the local Repeater/eUSB2/Controller may now be enabled for Peripheral operation. HostEnb and PeripheralEnb are mutually exclusive.

4.1.5 Signaling Modes

A eUSB2 Repeater at any given time operates in one of the two signaling modes (Figure 4-3):

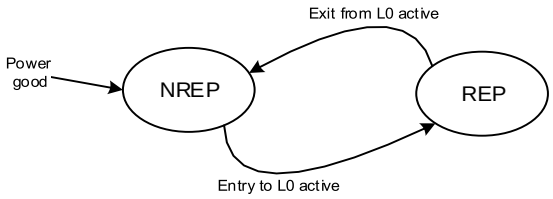


Figure 4-3: eUSB2 Repeater Operation Mode

- REP is a repeating signaling mode where packets are forwarded between eD+/eD- and D+/D-, with end to end timing preserved to meet the timing requirements defined by [USB 2.0] and eUSB2 specifications.

- NREP is a non-repeating signaling mode when the link is in one of the following states:
  - Initialization during Connect, Reset and Speed Negotiation.
  - L1 and Suspend.
  - L0 where a control message is being transmitted by local eDSPr/eUSPr to its associated Repeater.

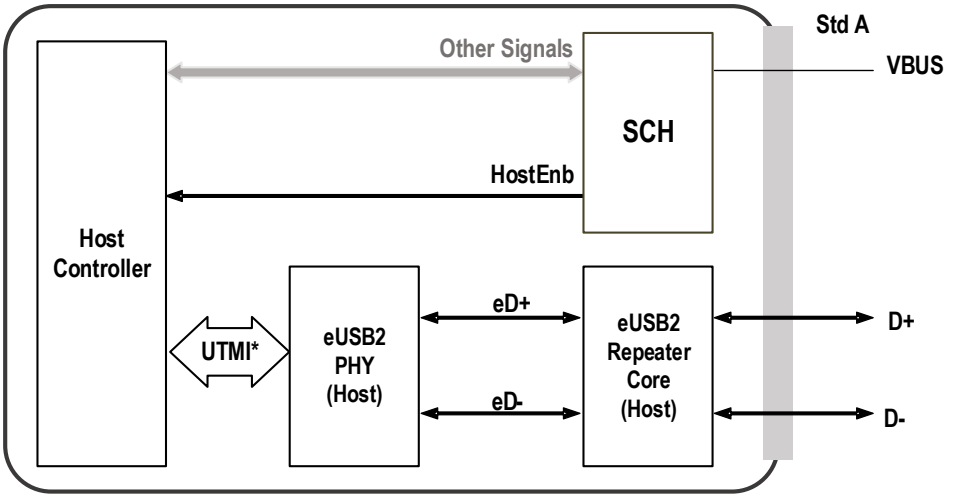
Timing in NREP mode is not as critical as REP since the information transmitted is for control and status reporting purposes such as Control Message, Chirp, or Repeater Configuration Announcement.

4.1.6 Operating Environment

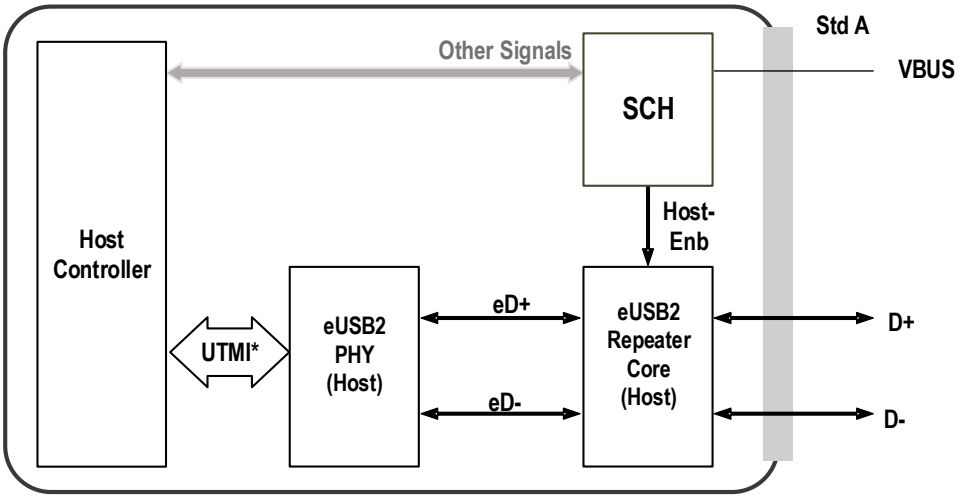
This section describes example configuration block diagrams between a eUSB2 repeater and its associated eDSPr/eUSPr and host and/or device controller under different operating environment.

4.1.6.1 Host Repeater

A eUSB2 Host Repeater bridges eUSB2 Host PHY (in SOC) and a USB2.0 downstream port at a Standard-A receptacle. An example of the operating environments under Top Down and Bottom Up schemes are illustrated in Figure 4-4.



(a) Host Repeater (Top Down)

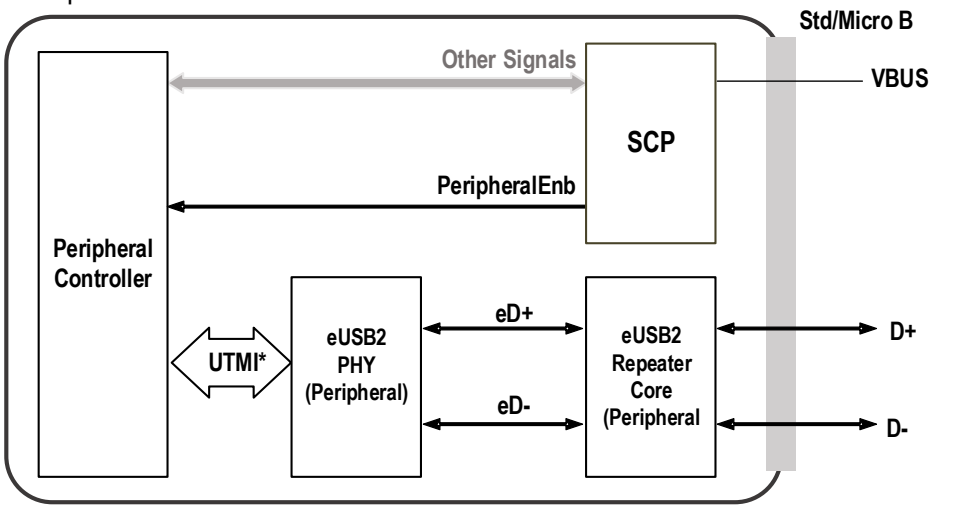


(b) Host Repeater (Bottom Up)

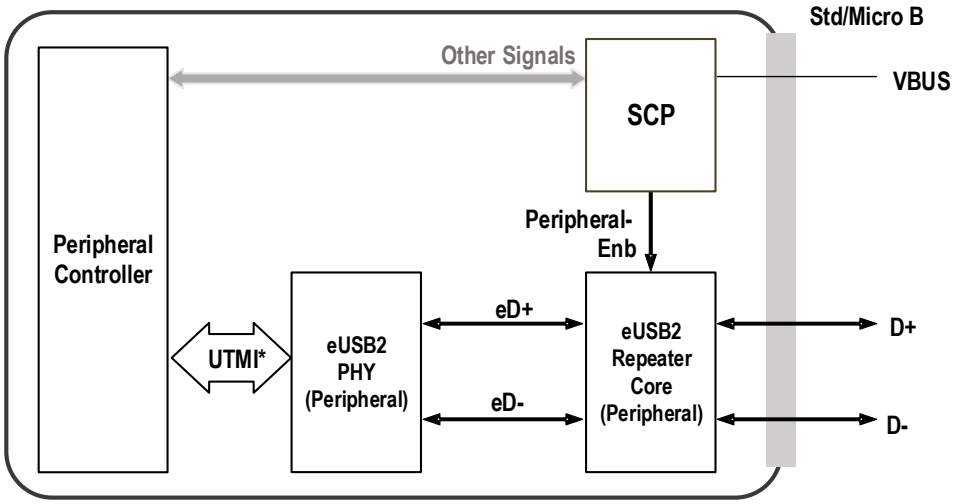
Figure 4-4: eUSB2 Host Repeater and its Operating Environment

4.1.6.2 Peripheral Repeater

A eUSB2 Peripheral Repeater extends a eUSB2 Peripheral PHY (in SOC) to a UUSP at a Standard-B or Micro-B receptacle. Figure 4-5 depicts its operating environment under Top Down and Bottom Up schemes.



(a) Peripheral Repeater (Top Down)



(b) Peripheral Repeater (Bottom Up)

Figure 4-5: eUSB2 Peripheral Repeater and its Operating Environment

4.1.6.3 DRD Repeater

A eUSB2 DRD Repeater bridges a eUSB2 DRD PHY (in SOC) and a USB2.0 DRD port (Micro--AB receptacle).

Such a eUSB2 DRD Repeater supports the so called Dual Role Function based on the following two cable types plugged into a Micro-AB receptacle:

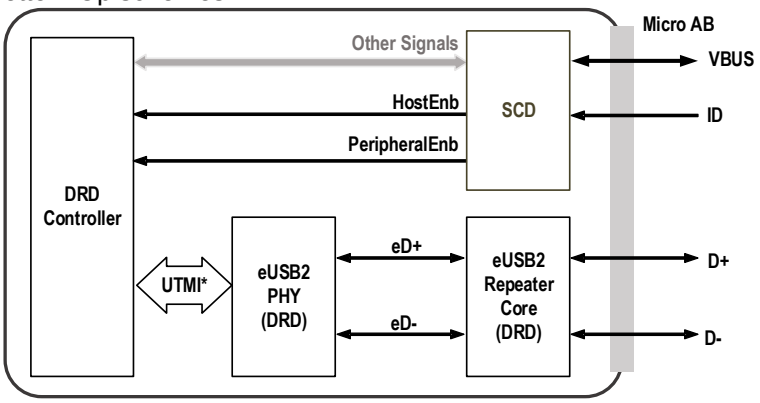
- Micro-B Plug to Standard-A
  - Micro-B Plug: mated with the local micro-AB receptacle of this DRD.
  - Standard-A: mated with a remote standard-A receptacle of a USB Host.

Under full OTG, the local controller behind Micro-AB receptacle is a B-Device. For DRD without the possibility of Role Swapping, it shall assume Peripheral mode operation.

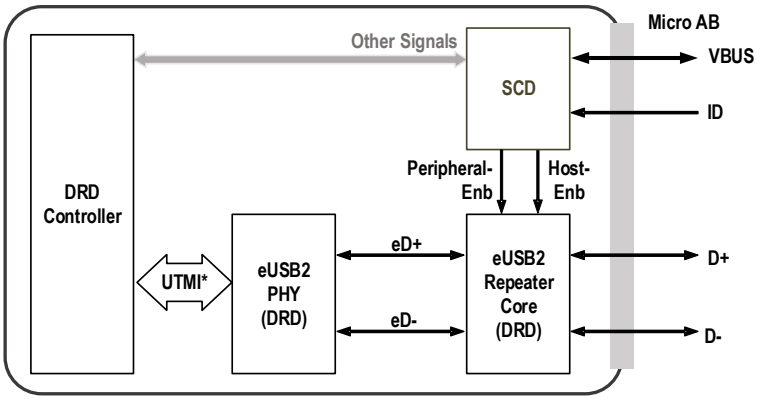
- Micro-A Plug to Standard-B/mini-B Plug
  - Micro-A Plug: mated with the local micro-AB receptacle of this DRD.
  - Standard-B/mini-B Plug: mated with a standard/mini-B receptacle of a USB Device.

Under full OTG, the local controller behind the micro-AB receptacle is an A-Device. For DRD without the possibility of Role Swapping, it shall assume Host mode operation.

Figure 4-6 depicts an example of the operating environments of a DRD eUSB2 Repeater under Top Down and Bottom Up schemes.



(a) DRD Repeater (Top Down)



(b) DRD Repeater (Bottom Up)

Figure 4-6: eUSB2 DRD Repeater and its Operating Environment

4.1.7 Repeater Implementation

Since Repeater implementation is vendor specific, the text in this section is entirely informative.

4.1.7.1 Repeater Implementation for USB Host

In addition to eUSB2 Host Repeater Core, a Repeater Implementation supporting USB Host may include part or all of a SCH:

- V_{BUS} Supplying circuit, such as a V_{BUS} Power Switch with Over Current detection, protection and reporting.
- Circuit to support Battery Charging if desirable.

Output signal HostEnb is:

- Asserted only after V_{BUS} power is reliably established, and Battery Charging handshake has been completed.
- De-asserted if V_{BUS} over current is detected; or directed by Host Controller.

4.1.7.2 Repeater Implementation for USB Peripheral

In addition to eUSB2 Peripheral Repeater Core, a Repeater Implementation supporting USB Peripheral may include part or all of a SCP:

- V_{BUS} Qualification circuit (for instance, level shifting and de-bouncing).
- Battery Charging if desired.

Output signal PeripheralEnb is:

- Asserted only after V_{BUS} is fully qualified and Battery Charging handshake has been completed.
- De-asserted if V_{BUS} is no longer valid.

4.1.7.3 Repeater Implementation for USB DRD

In addition to eUSB2 DRD Repeater Core, a Repeater Implementation that supports USB DRD may include part or all of a SCD:

- DRD Role Logic.
- ID pull-up and de-bouncing.
- V_{BUS} Switch and Over Current Detection for host mode operation.
- V_{BUS} Qualification circuit (level shifting and de-bouncing) for peripheral mode operation.
- Battery Charging (for host and peripheral) if desired.

Output signal HostEnb is:

- Asserted only after ID = False is detected, V_{BUS} power is reliably established, and Battery Charging handshake (if there) has been completed.
- De-asserted if V_{BUS} over current is detected, directed by DRD Controller, or ID = T is detected.

Output signal PeripheralEnb is:

- Asserted only after ID = True and V_{BUS} is fully qualified and Battery Charging handshake has been completed.
- De-asserted if V_{BUS} is no longer valid.

4.1.7.4 A Repeater Implementation Example

Figure 4-7 depicts a eUSB2 Repeater Implementation for mobile platforms:

- Supports DRD (Bottom Up) and optional OTG.
- Supports Battery Charging (BC), Accessory Charging Adapter (ACA), Host Power Switch, etc. in a standalone repeater or integrated in PMIC.

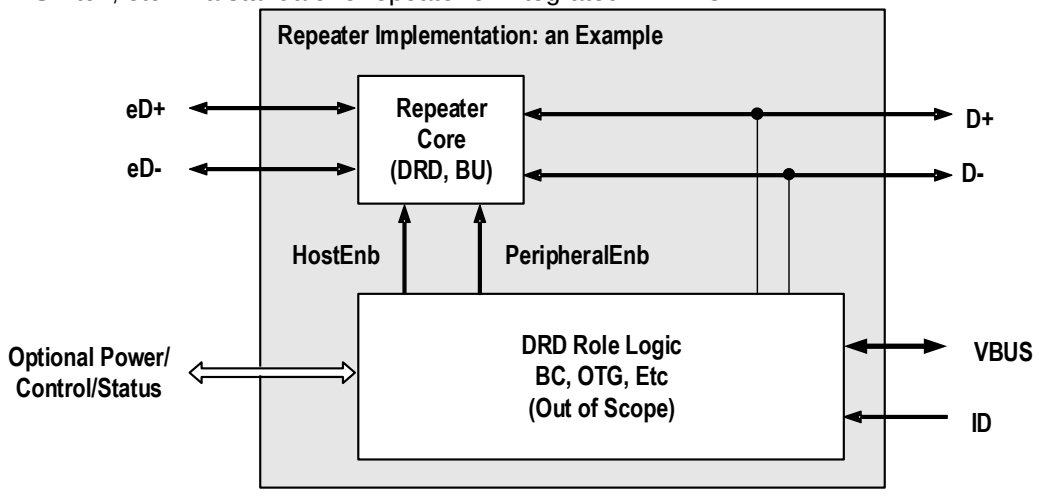


Figure 4-7: An Example of eUSB2 Repeater Product Supporting (DRD, BU)

Note that:

- In this example, a BU scheme is employed. HostEnb and PeripheralEnb are inputs to the Repeater Core. Note that if TD scheme is employed, HostEnb and PeripheralEnb would become output pins of this Repeater Implementation.
- The configuration of a complex Repeater Implementation can be made via RAP described in Chapter 5, though not shown in the figure.

4.2 *Repeater Core Operation*

In the rest of this chapter, unless explicitly stated, Repeater refers to a Repeater Core.

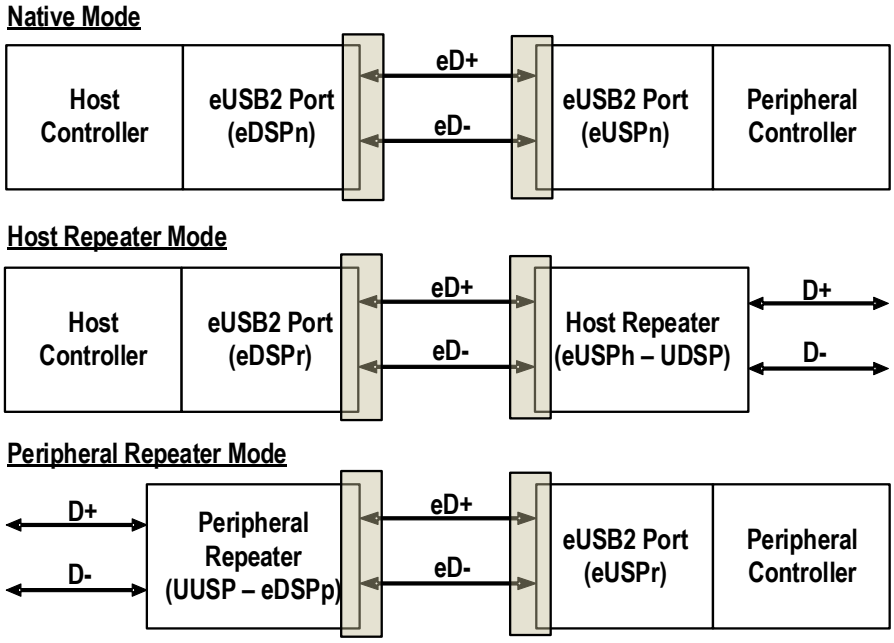


Figure 4-8: eUSB2 Port Naming Convention in Native Mode and Repeater Mode.

4.2.1 Host Repeater

The operation of a eUSPh is the same as a eUSPn, except for the following:

- It shall complete repeater TBConfig as defined in Section 4.2.5.
- It shall perform USB2.0 device disconnect while the link is in L1 and L2. Refer to Sections 4.2.7.2 and 4.2.7.5 for details.
- It shall perform device disconnect announcement when operating under Bottom Up configuration.
- It shall perform entry to L1/L2 based on CM.L1/CM.L2 issued by its eDSPr.
- It shall manage HS disconnect detect upon entry to L2 based on CM.Detect received from its eDSPr. Refer to Section 4.2.7 for details.
- It is not required to transmit digital/analog ping in L0 to indicate device and host repeater presence. The eDSPr shall not perform device disconnect detection based on digital/analog ping. Note that the host repeater will always report USB2.0 device disconnect in any link state.
- It may transmit the LS/FS EOP as defined in Section 3.4.2, which is different from native mode. The eDSPr shall expect alternative LS/FS EOP as compared to that in native mode.
- It may optionally monitor the SE0 idle duration for detection of sudden removal of an eDSPr. Note that although highly undesirable, implementation may exist that an eDSPr is powered down without proper power-off sequencing. A Host repeater in HS operation

may remain in L0 without entering L2 and therefore switch to FS. Under this situation, a USB2.0 device may loop through Reset, speed detection, device switching to FS due to lack of the host chirp acknowledgement and reset. To avoid this undesired behavior, a Host repeater may monitor the SE0 at eD+/eD- with its local clock, and transition to L2 upon detecting link idle for more than 3ms.

Likewise, the operation of an eDSPr is the same as an eDSPn except as described above.

4.2.2 Peripheral Repeater

The operation of an eDSPp is the same as an eDSPn, except the following:

- It shall complete repeater TBConfig as defined in Section 4.2.5.
  It shall manage L1 and L2 entry based on CM.L1/CM.L2 in LS/FS operation. Refer to Section 4.2.7 for details.
- It shall manage L2 entry and L2/reset differentiation in HS operation based on CM.Zero. Refer to Section 4.2.7 for details.
- If shall perform reset detection based on its local clock in LS/FS operation, or when the link is L1/L2. Note that the operation is the same as native mode except the reset declaration is based on observing SE0 at USB2.0 bus for more than 2.5us.
- It shall manage its HS receiver termination control with assistance from the eUSPr.
- It shall perform the eUSB2 device disconnect in L0 based on digital/analog ping.
- It shall perform host disconnect announcement when operating under Bottom Up configuration. Refer to Section 4.2.7.6 for details.

Likewise, the operation of a eUSPr is the same as a eUSPn except as described above.

4.2.3 DRD Repeater

A eUSB2 DRD Repeater operating in host or peripheral mode is the same as a Host Repeater or a Peripheral Repeater respectively.
In addition, a DRD repeater shall implement at least one of the following configuration schemes:

- Top Down: Operate in host or peripheral repeater mode according to CM.Host or CM.Peripheral, and CM.Default. Refer to Section 4.1.3 for details.
- Bottom Up: Generation of Host Announcement, Peripheral Announcement, and Disconnect signaling based on status of HostEnb and PeripheralEnb.

4.2.4 Repeater Reset

Repeater reset refers to power-on reset or HW reset. Note that HW reset is implementation specific. A repeater shall perform one of the following:

- It shall transmit a repeater presence announcement at its eUSB2 port.
- It shall disable its transceiver at its USB2.0 port.
- It shall perform TBConfig as defined in Section 4.2.5.
- Upon completion of TBConfig, it shall perform one of the following:
  - If it is a host repeater with TD configuration, it shall wait until it has received CM.Host before enabling its downstream USB2.0 port in expectation of a USB2.0 device connect. Else if it is a host repeater with BU configuration, it shall wait until it has detected the assertion of HostEnb before enabling its downstream USB2.0 port in expectation of a USB2.0 device connect.
  - If it is a peripheral repeater with TD configuration, it shall wait until it has received CM.Peripheral before enabling its downstream eUSB2 port in expectation of a eUSB2 device connect. Else if it is a Peripheral repeater with BU configuration, it shall wait until it has detected the assertion of PeripheralEnb before enabling its downstream eUSB2 port in expectation of a eUSB2 device connect.

4.2.5 eUSB2 Repeater TBConfig

Note: An implementation may choose alternative ways of communication between an eUSB2 repeater and an eDSPr/eUSPr to achieve the following configuration. Therefore, implementation of the TBConfig method described in this section in optional.

eUSB2 repeater TBConfig refers to synchronization with its associated eDSPr/eUSPr deciding Top Down or Bottom Up configuration before start of the repeater operation.

- A eUSB2 repeater shall perform TBConfig upon power-up. This includes a eUSB2 repeater which is either preconfigured, or capable of only single configuration.
- A eUSB2 repeater shall adhere to the following rules:
    - Upon completing repeater presence announcement, it shall wait for TBConfig from its associated eDSPr/eUSPr.
    - Upon detecting logic '1' at eD+ for $T_{TBConfig}$, it shall transmit an acknowledgement at eD- and declare Top Down configuration.
    - Upon detecting logic '1' at eD- for $T_{TBConfig}$, it shall transmit an acknowledgement at eD+ and declare Bottom up configuration.
- A eUSB2 port shall adhere to the following rules:
    - Upon completing DSP reset announcement, or USP presence announcement, it shall initiate TBConfig if it has observed SE0 at eUSB2 bus for T_{IDLE}. Note if it is DRD eUSB2 port, it may transmit either DSP reset announcement or USP presence announcement.
    - It shall drive logic '1' at eD+ for Top Down configuration. It shall conclude TBConfig if it has detected the acknowledgement from its eUSB2 repeater at eD-. It shall drive logic '0' at eD+ upon detecting the conclusion of repeater acknowledgement. Note that if it has detected the duration of eD- is two times longer than the maximum T_{ACK}, it shall stop driving eD+ and check if either a DSP reset announcement or USP presence announcement is received.
    - It shall drive logic '0' at eD- for Bottom Up configuration. It shall conclude TBConfig if it has detected the acknowledgement from its eUSB2 repeater at eD+. It shall drive logic '0' at eD- upon detecting the conclusion of repeater acknowledgement. Note that if it has detected the duration of eD+ is two times longer than the maximum T_{ACK}, it shall stop driving eD- and check if either a DSP reset announcement or USP presence announcement is received.

Shown in Figure 4-9 is an example of TBConfig. Note that it is the implementation's responsibility to make sure that an eDSPr/eUSPr and its associate eUSB2 repeater are capable of common TBConfig.

For Figure 4-9 (a):

At t0, the eUSB2 port powers up. Note that in this example, it is assumed that the eUSB2 repeater has already powered-up earlier and has completed repeater presence announcement.

At t1, after observing SE0 for T_{IDLE}, the eUSB2 port starts transmitting a port reset announcement.

At t2, the eUSB2 port concludes the port reset announcement.

At t3, after observing SE0 for T_{IDLE}, the eUSB2 port start TBConfig by driving Logic "1" at eD+ to configure the eUSB2 repeater to Top Down configuration.

At t4, after observing logic '1' at eD+ for $T_{TBConfig}$, the eUSB2 repeater drives logic '1' at eD- to acknowledge the TBConfig.

At t5, the eUSB2 repeater concludes TBConfig. The eDSPr/eUSPr and its associated eUSB2 repeater conclude Top Down configuration and are ready for USB operation.

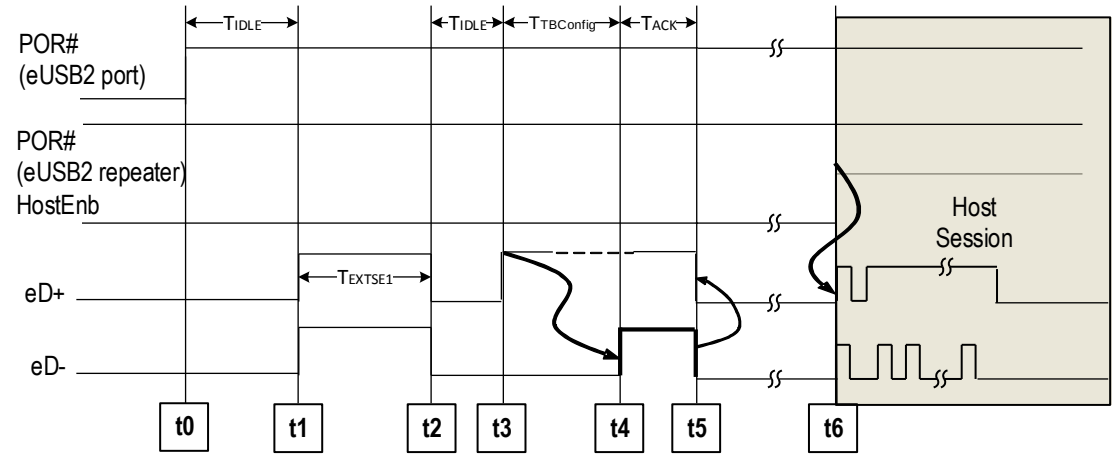
At t6, HostEnb is asserted by the SCH/SCD. The eUSB2 port issues CM.Host. The host session starts.

For Figure 4-9 (b):

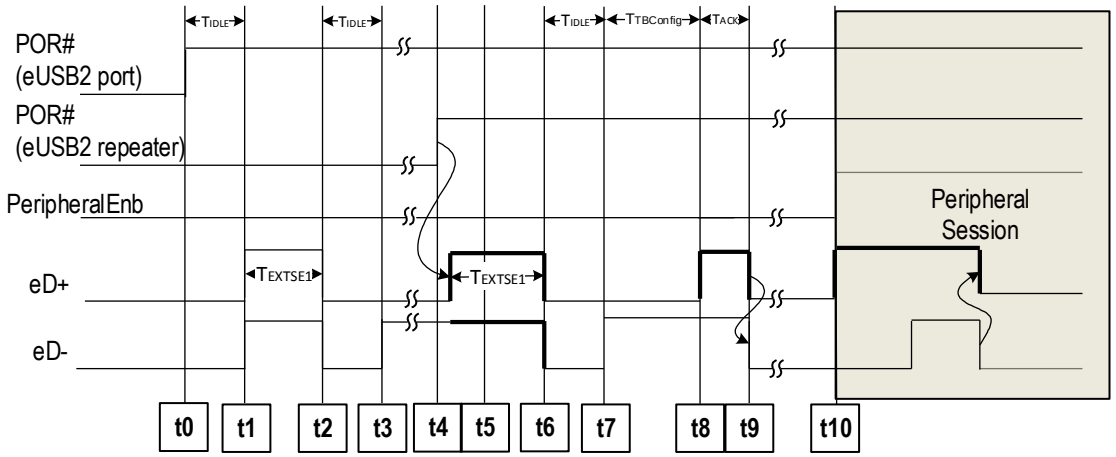
At t0, the eUSB2 port powers up.

At t1, after observing SE0 for T_{IDLE}, the eUSB2 port starts transmitting a port reset announcement.
At t2, the eUSB2 port concludes the port reset announcement.
At t3, after observing SE0 for T_{IDLE}, the eUSB2 port start TBConfig by driving Logic “1” at eD- to configure the eUSB2 repeater to Bottom Up configuration.
At t4, the eUSB2 repeater powers up and issues the repeater presence announcement regardless of the state at its eUSB2 bus.
At t5, after observing logic ‘1’ at eD+ for more than the maximum of T_{ACK}, the eUSB2 port retrieves TBConfig by disabling its transmitter. It continues to observe SE1, the eUSB2 port declares the reception of the repeater presence announcement.
At t6, the eUSB2 repeater concludes repeater presence announcement.
At t7, upon observing conclusion of the repeater presence announcement for T_{IDLE}, the eUSB2 port restarts TBConfig.
At t8, after observing logic ‘1’ at eD- for $T_{TBConfig}$, the eUSB2 repeater drives logic ‘1’ at eD+ to acknowledgment TBConfig.
At t9, the eUSB2 repeater concludes TBConfig. The eDSPr/eUSPr and its associated eUSB2 repeater conclude Bottom Up configuration and are ready for USB operation.
At t10, PeripheralEnb is asserted by SCP/SCD. The eUSB2 repeater announces micro-B plug event. The peripheral session starts.

Note: as can be seen from the example, the nature of asynchronous power-up between an eDSPr/eUSPr and its associated eUSB2 repeater, a eUSB2 repeater may miss the complete or partial DSP reset announcement from its eUSB2 port. Similar situation applies to a eUSB2 port. It is to be noted that both the eDSPr/eUSPr and its associated eUSB2 repeater shall expect those scenarios and perform TBConfig accordingly.



(a) Top Down Repeater Configuration: Host Repeater



(b) Bottom Up Repeater Configuration: Peripheral Repeater

Figure 4-9: Example eUSB2 Repeater TBConfig

4.2.6 Repeater Bus State and Signaling

- The USB2.0 port (D+/D-) of the eUSB2 repeater shall meet bus state and signaling requirements outlined in [USB2.0].
- The eUSB2 port (eD+/eD-) of the repeater shall meet electrical and timing requirements specified in this document.

4.2.7 Repeater Specific Control Messaging and Signaling

In addition to CM.Reset that is employed in both native and repeater mode operation, control messages are defined to assist the repeater operation based on a relaxed clock with +/-50% tolerance.

4.2.7.1 CM.L1

- CM.L1 is defined for an eDSPr or eUSPr to inform its associated host or peripheral repeater about entry to L1. A eUSB2 downstream port shall transmit CM.L1 to its host repeater within $T_{L1TokenRetry}$ (min) as defined by the LPM-L1 addendum.
- A eUSPr or eUSPh, upon sending L1 token acknowledgment, shall start transmitting CM.L1 to its peripheral repeater no earlier than $T_{L1TokenRetry}$ (min) and no later than $T_{L1TokenRetry}$ (max) as defined by the LPM-L1 addendum.

- A repeater, upon receiving CM.L1, shall enter L1 within the minimum L1 residency time defined by the LPM-L1 addendum.

4.2.7.2 CM.L2

CM.L2 is defined for an eDSPr to inform its associated host repeater about entry to L2. It is also used for a eUSPr to inform its associated peripheral repeater about entry to L2 in LS/FS operation. Refer to Section 4.2.7.3 for specific operation regarding a eUSPr or eUSPh in HS operation directing its peripheral repeater regarding entry to L2.

- An eDSPr/eUSPr shall transmit CM.L2 to its associated repeater upon L2 entry.
- A eUSB2 repeater, upon receiving CM.L2, shall enter L2 meeting requirement defined by [USB2.0].

4.2.7.3 CM.Zero

CM.Zero is defined specifically for eUSPr or eUSPh to direct its peripheral repeater in differentiating between L2 entry and USB2.0 bus reset when in HS operation.
In HS operation, the entry to L2 is detected by a USB2.0 device switching from HS termination to FS termination upon detecting SE0 idle for 3ms. If the line state changes to FS J, it indicates the host USB2.0 port is suspended. Otherwise, if SE0 persists, it indicates that the host USB2.0 port is driving a USB2.0 bus reset. To facilitate the differentiation between L2 entry and USB2.0 bus reset, a eUSPr and its associate peripheral repeater shall perform the following upon detecting link idle for 3ms:

- Upon detecting link idle for 3ms, a eUSPr or eUSPh port shall transmit CM.Zero to its peripheral repeater within 125us.
- Upon receiving CM.Zero, a eUSB2 peripheral repeater shall switch its transceivers from HS to FS, then sample the line state. It shall perform one of the following:
    - If it has detected the line state changed from SE0 to J, it shall transmit a digital ping at eD- within 50us upon detecting CM.Zero.
    - If it has detected the line state unchanged as SE0, it shall remain in this state.
- A eUSPr or eUSPh, upon issuing CM.Zero, shall sample eD- within 100us. It shall declare one of the following:
    - If it has detected the digital ping at eD-, it shall declare the entry to L2.
    - If it has not detected the digital ping at eD-, it shall declare USB2.0 bus reset is detected.

Shown in Figure 4-10 and Figure 4-11 are example timing diagrams of a eUSPr directing the eDSPp in identifying between USB2.0 bus reset and entry to suspend. Note that the control signals from the UTMI+ interface at host and device eUSB2 port are referenced.

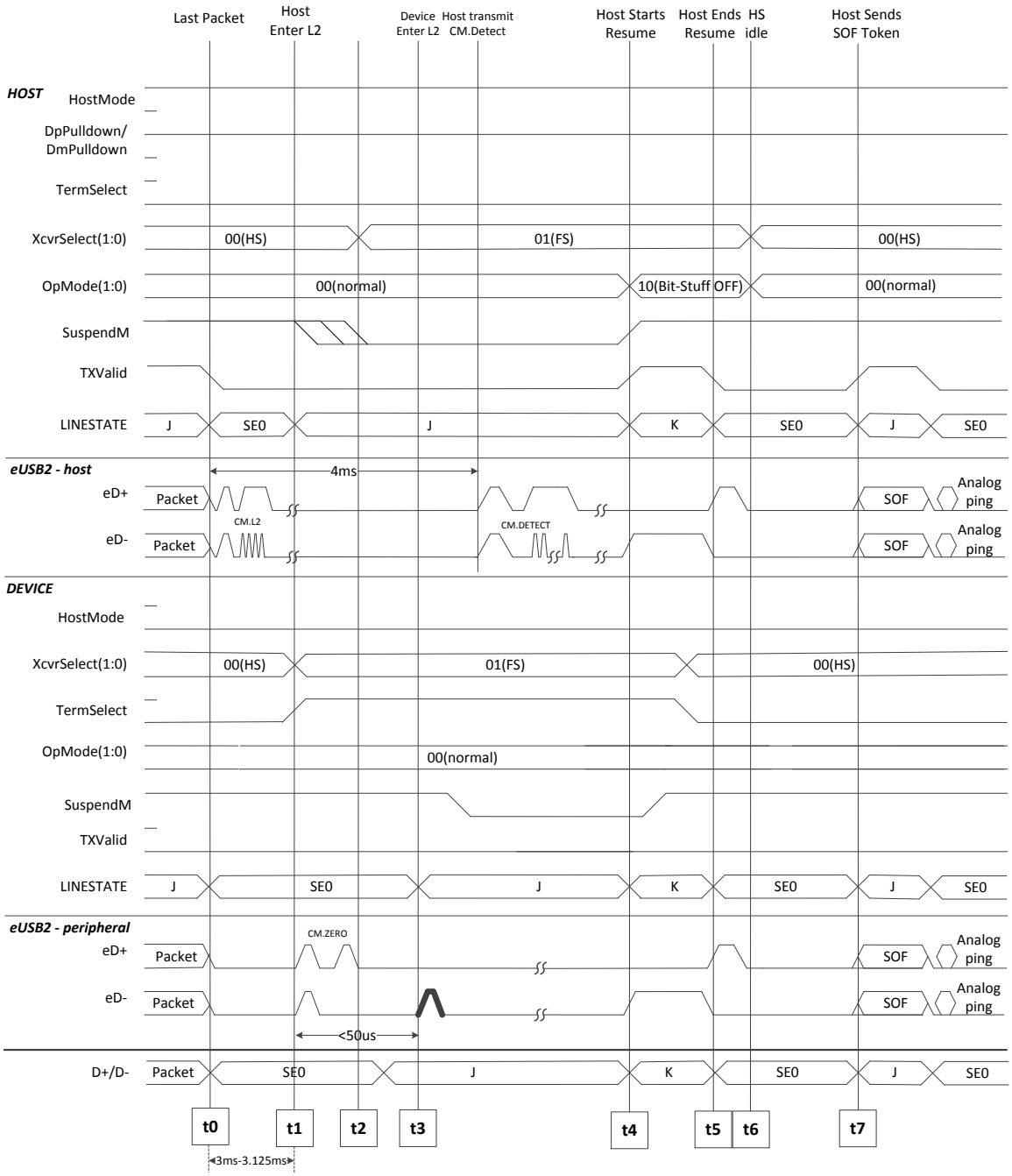


Figure 4-10: Example of eUSPr Directing its Peripheral Repeater in Detection and Entry to L2

At t0, eDSPr issues CM.L2 to direct its host repeater to L2. The USB2 bus state is SE0.
At t1, eUSPr issues CM.Zero after detecting link idle for 3-ms. It also starts a 100-us timer.
At t2, upon detecting CM.Zero, the peripheral repeater configure its transceiver to FS and performs USB2 bus state detection.
At t3, eDSPp issues a digital ping to eUSPr to inform the USB2 bus state change to Idle J. both eDSPp and eUSPr enter L2.

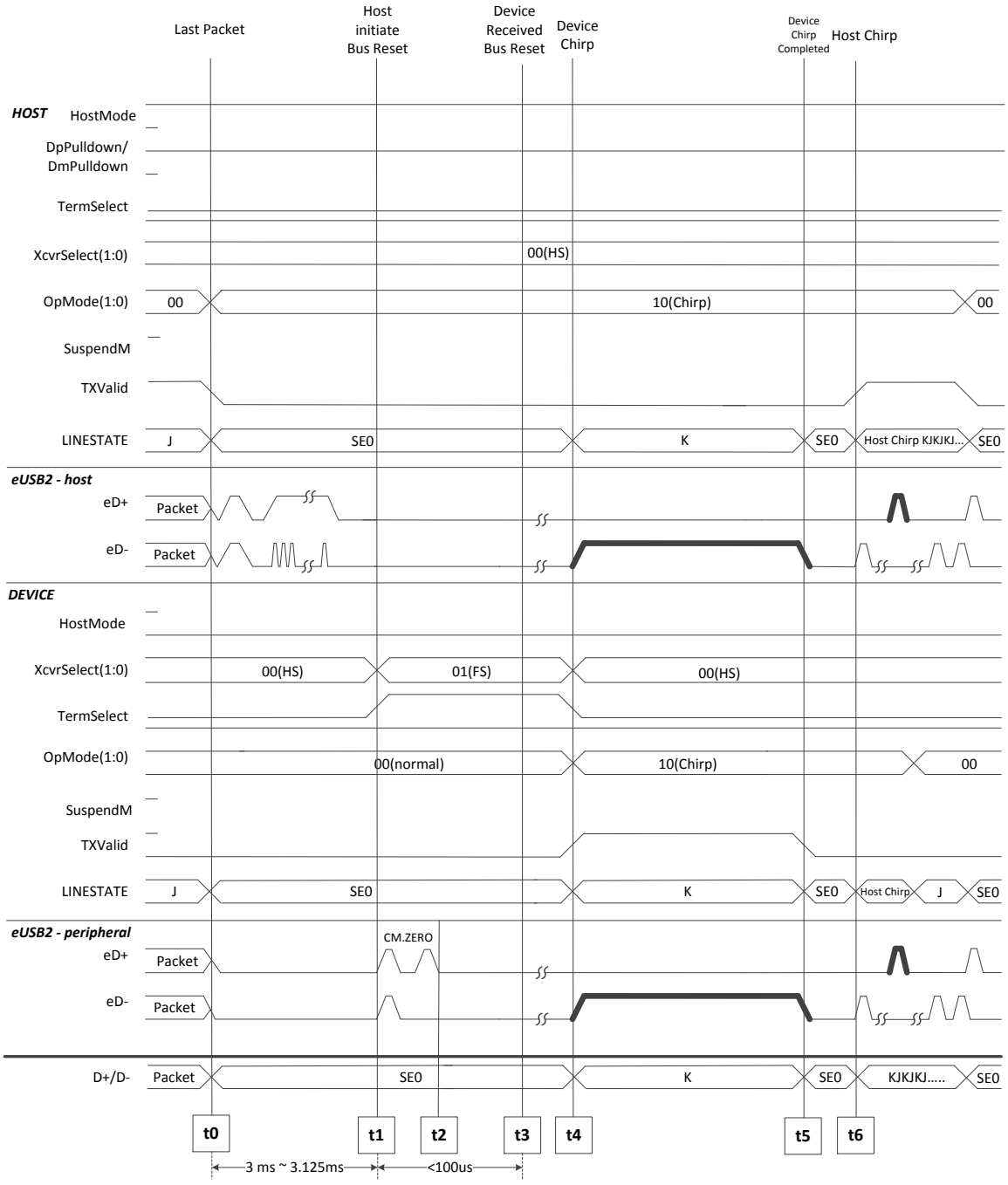


Figure 4-11: Example of eUSPr Directing its Peripheral Repeater in Detection Reset

At t0, eDSPr issues CM.L2 to direct its host repeater to L2. The USB2 bus state is SE0.
At t1, eUSPr issues CM.Zero after detecting link idle for 3-ms. It also starts a 100-us timer.
At t2, upon detecting CM.Zero, the peripheral repeater configure its transceiver to FS and performs USB2 bus state detection.
At t3, eUSPr does not receiver the digital ping from eDSPp within 100-us. It declares USB2 bus reset.
At t4, eUSPr issues Chirp K to start high-speed detection.

4.2.7.4 CM.Detect

CM.Detect applies only to the host repeater in HS operation upon entry to L2.
Upon entering L2, the line state (D+/D-) of a host repeater in HS will transition from SE0 to D+ pull-up. As a downstream port and its upstream link partner may not switch to FS synchronously, the line state at the USB2.0 bus may remain in SE0 before both ports are in FS. To prevent a downstream port from declaring device disconnect during this transition period, a host repeater shall disable its device disconnect detect until a predetermined time that L2 entry is ensured based on USB2.0 protocol requirement.

- An eDSPr shall implement a disconnect recover timer ($T_{L2DiscRec}$), and start this timer upon entry to L2. Refer to Section 2.2.1.10 of [UTMI+ v1.0] for details.
- Upon the expiration of $T_{L2DiscRec}$ timer, an eDSPr shall transmit CM.Detect to its associate host repeater to start disconnect detect.
- A host repeater, upon detecting CM.L2, shall disable its device disconnect detection at USB2.0 bus while transitioning to L2.
- A host repeater, upon detecting CM.Detect, shall enable its device disconnect detection.

4.2.7.5 Disconnect Detect in L1 Suspend

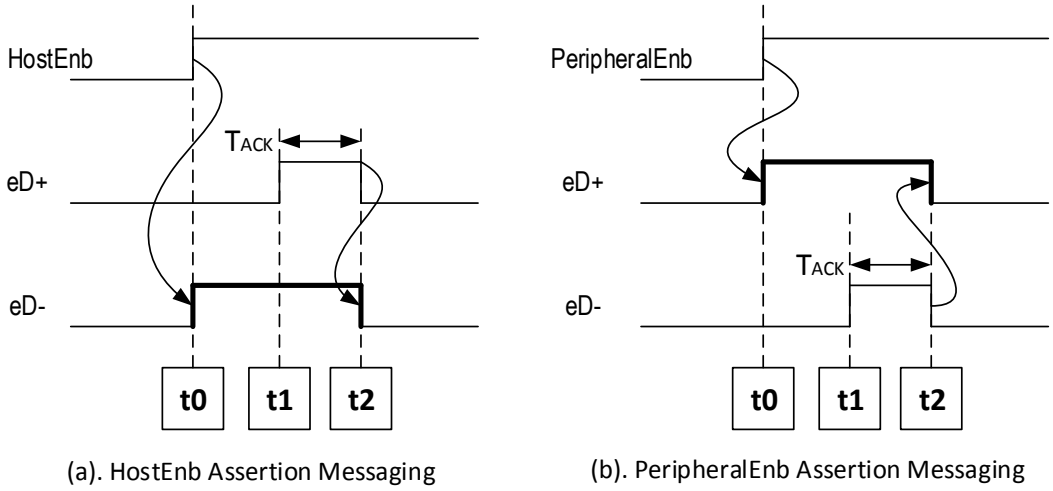
The mechanism for managing disconnect detect in L1 while eUSB2 was operating in HS is similar to that in L2, with the exception that the disconnect recovery timer is implemented at the host repeater. This is primarily due to the facts that the minimum L1 residency is relative, and an USB2.0 device is only required to be in L1 with the entry latency to be within the minimum L1 residency. This may lead to potential contention between CM.Detect and device remote wake. To avoid this potential corner case, the following rules shall apply to a host repeater:

- Upon detecting CM.L1, it shall enable a L1 disconnect recover timer ($T_{L1DiscRec}$) and continue to monitor the line state at its USB2.0 bus.
- It shall declare device disconnected if both of the following conditions are met.
    - The $T_{L1DiscRec}$ timer has expired.
    - The line state has transitioned to J from SE0.

4.2.7.6 HostEnb/PeripheralEnb Messaging

HostEnb/PeripheralEnb Messaging applies only to Bottom Up configuration. It is employed by a eUSB2 repeater to inform its associate eDSPr/eUSPr about the assertion of HostEnb/PeripheralEnb.

- Shown in Figure 4-12 (a), the eUSPh of the host repeater and eDSPr shall perform the following to deliver the message of HostEnb assertion:
    - Upon detecting the assertion of HostEnb, the eUSPh shall drive logic ‘1’ at eD-.
    - Upon detecting logic ‘1’ at eD-, the eDSPr shall drive an acknowledgement at eD+.
    - Upon detecting the conclusion of the acknowledgement from eDSPr, the eUSPh shall drive logic ‘0’ at eD- to conclude the message of HostEnb assertion.
- Shown in Figure 4-12 (b), the eDSPp of the peripheral repeater and eUSPr shall perform the following to deliver the message of PeripheralEnb assertion:
    - Upon detecting the assertion of PeripheralEnb, the eDSPp shall drive logic ‘1’ at eD+.
    - Upon detecting logic ‘1’ at eD+, the eUSPr shall drive an acknowledgement at eD-.
    - Upon detecting the conclusion of the acknowledgement from eUSPr, the eDSPp shall drive logic ‘0’ at eD+ to conclude the message of PeripheralEnb assertion.
    - Upon detection of the de-assertion of HostEnb, the eUSPh shall issue a device disconnect announcement to the eDSPr.
    - Upon detection of the de-assertion of PeripheralEnb, the eDSPp shall issue a host disconnect announcement to the eUSPr.



(a). HostEnb Assertion Messaging (b). PeripheralEnb Assertion Messaging

Figure 4-12: Example HostEnb/PeripheralEnb Assertion Messaging (BU)

4.2.8 Repeater Session

A repeater session refers to a USB session from the start where a connect event is detected to the end where a disconnect event is detected.

- A eUSB2 repeater shall first complete TBConfig before it can accept a repeater session.
- A peripheral repeater session shall be started if the following three conditions are met:
  - The eUSB2 repeater is capable of peripheral repeater mode.
  - PeripheralEnb is asserted and communicated to the repeater based on one of the following:
    - Top Down configuration: CM.Peripheral is received.
    - Bottom Up configuration: detection of PeripheralEnb assertion and the PeripheralEnb assertion messaging has been sent.
  - The eUSB2 repeater has enabled its eUSB2 port to start the USB session.

Figure 4-13 is the timing diagram of a eUSB2 Repeater operating under Top Down scheme from the assertion of PeripheralEnb to USB2.0 Reset.

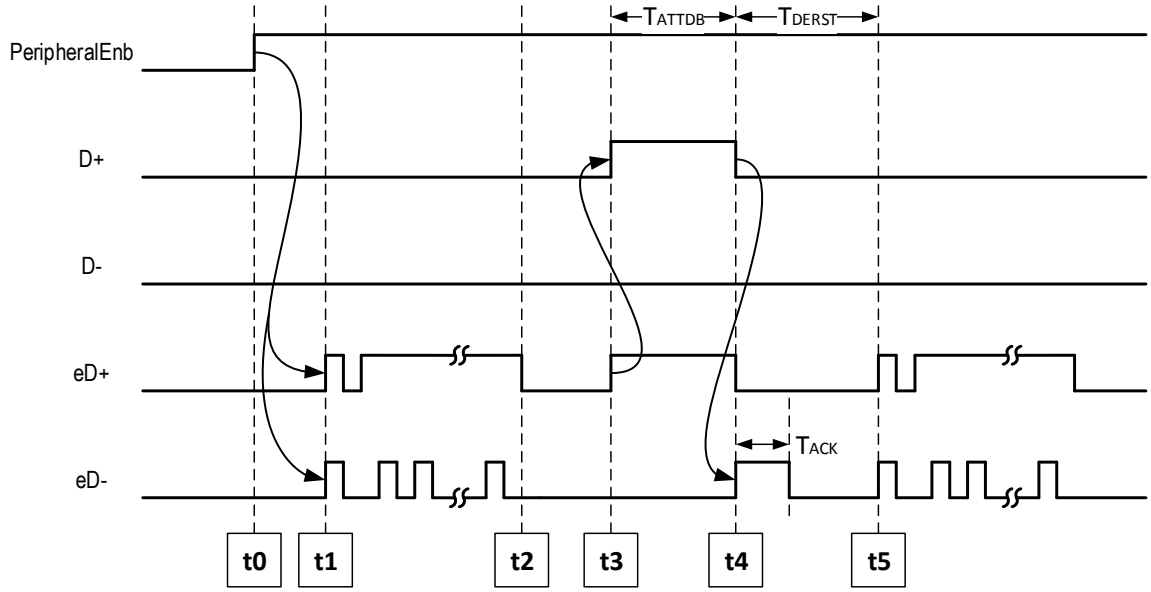


Figure 4-13: Repeater Operation upon Assertion of PeripheralEnb (Top Down)

At t0, PeripheralEnb is asserted to the Controller, which then passes this information to its eUSB2 port.
At t1, the eUSB2 port sends CM.Peripheral to the Repeater.
At t2, the Repeater has received CM.Peripheral. It is now ready to receive device connect from its associate eDSPr/eUSPr.
At t3, the eUSB2 port drives Logic "1" at eD+ to indicate a device connect. The Repeater then enable its pull-up resistor at D+. (If the peripheral is low speed, Repeater enables its pull-up at D-).
At t4, the Repeater observes SE0 at D+/D- (USB2 Reset by Host), and drives an acknowledgement at its eUSB2 port.
At t5, SE0 is detected for more than 2.5 us, the Repeater issues CM.Reset to its associate eDSPr/eUSPr.

The figure below is the timing diagram of a eUSB2 Repeater operating under Bottom Up scheme from the assertion of PeripheralEnb to USB2.0 bus reset.

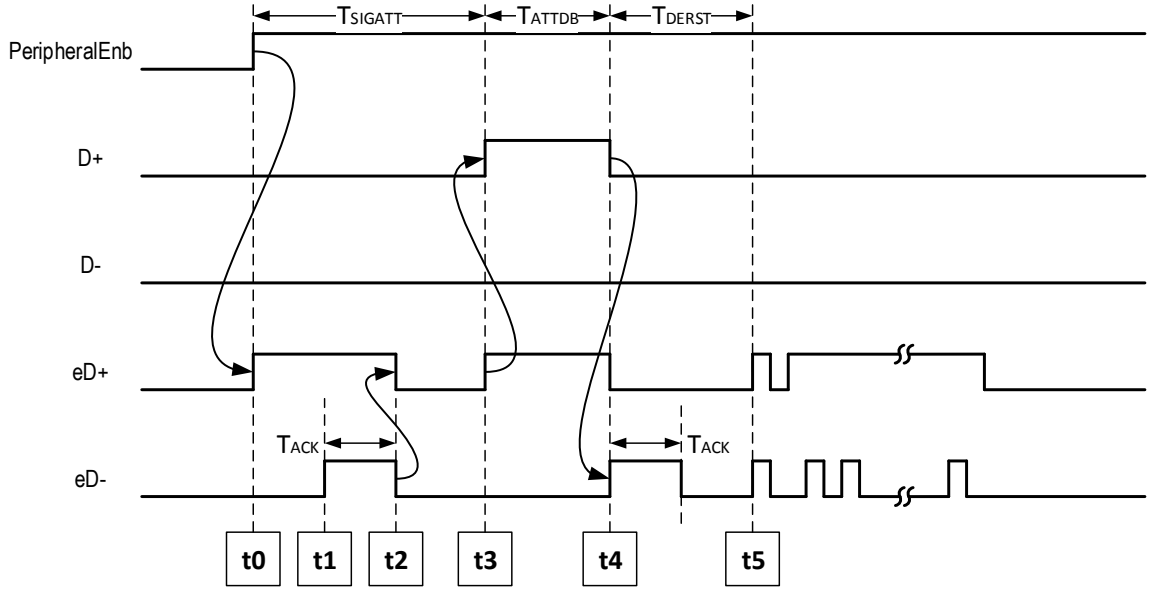


Figure 4-14: Repeater Operation upon Assertion of PeripheralEnb (Bottom Up)

At t0, the Repeater detects assertion of PeripheralEnb (BU). It drives Logic "1" at eD+ to pass this information to its associate eDSPr/eUSPr.
At t1, the eUSB2 port drives an acknowledgement at eD-.
At t2, the eUSB2 port concludes acknowledgment and observes eD+ remaining at Logic "1". The Repeater, upon detecting logic "0" at eD-, drives logic '0' at eD+ and disables its SE transmitter. It then enables its SE receivers at eD+ and eD-. The peripheral is now ready to receive device connect from its associate eDSPr/eUSPr.
At t3, the eUSB2 port drives Logic "1" at eD+ to indicate a device connect. The Repeater then enable its pull-up resistor at D+. (If the peripheral is low speed, Repeater enables its pull-up at D-).
At t4, the Repeater observes SE0 at D+/D- (USB2 Reset by Host), and drives an acknowledgement at its eUSB2 port.
At t5, SE0 is detected for more than 2.5us, the Repeater issues CM.Reset to its associate eDSPr/eUSPr.

- A host repeater session shall be started if the following three conditions are met:
  - The eUSB2 repeater is capable of host repeater mode.
  - HostEnb is asserted and communicated to the repeater based on one of the following:

- Top Down configuration: CM.Host is received.
- Bottom Up configuration: detection of HostEnb assertion and the HostEnb assertion messaging has been sent.

○ The eUSB2 repeater has enabled its USB2.0 port to start the USB session.

Figure 4-15 is the timing diagram of a eUSB2 Repeater operating under Bottom Up scheme from the assertion of HostEnb to USB2.0 Reset.

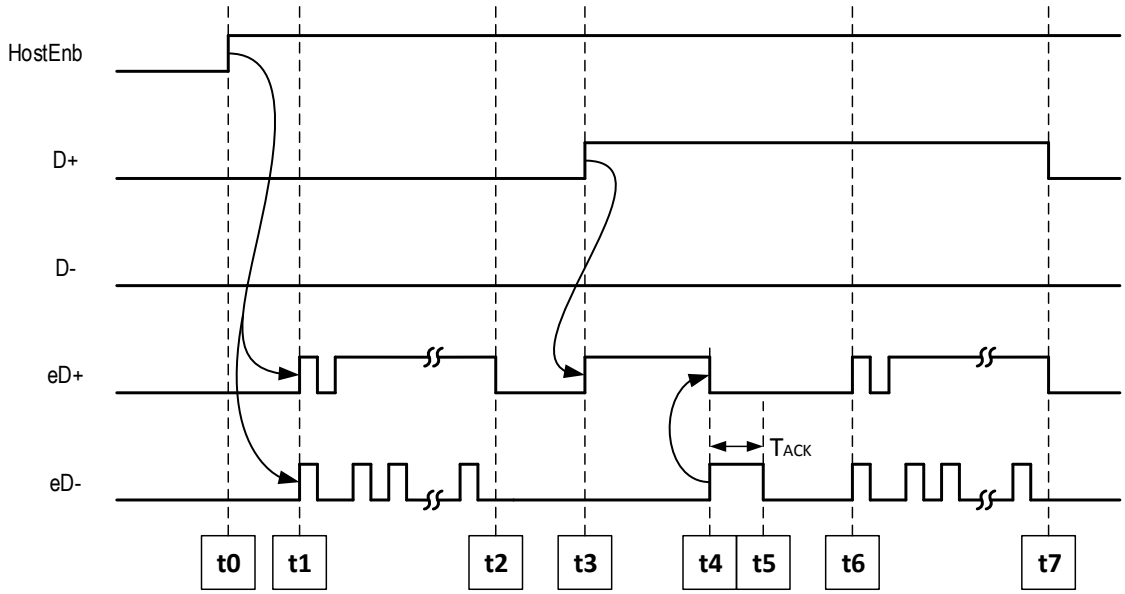


Figure 4-15: Repeater Operation upon Assertion of HostEnb (Top Down)

At t0, HostEnb is asserted at the Controller.
At t1, upon observing SE0 for T_{IDLE}, the eDSPr issues CM.Host to its associated eUSB2 host repeater.
At t2, the eUSB2 repeater received CM.Host. Both pull-down resisters are turned on at D+/D-. The Host is ready for USB2.0 device connect.
At t3, a J state at D+/D- indicates a connection of a USB2.0 device. The Repeater then announces this connection by driving eD+ to Logic "1". (If a low speed device is connected, eD- shall be driven instead.)
At t4, the eDSPr acknowledges device connect at eD-. Repeater stops driving Logic "1" at eD+. (If a low speed device was connected, acknowledgement by the eDSPr will be on eD+, and Repeater stops driving Logic "1" on eD- instead).
At t5, the eDSPr's acknowledgement on device connection is concluded. Repeater shall turn on its eD+/eD- receiver.
At t6, the eDSPr issues CM.Reset to its associate repeater.
At t7, the Repeater detects CM.Reset. It then asserts HS terminations at D+/D- , and issues USB2.0 bus reset.

Figure 4-16 is the timing diagram of a eUSB2 Repeater operating under Bottom Up scheme from the assertion of HostEnb to USB2.0 bus reset.

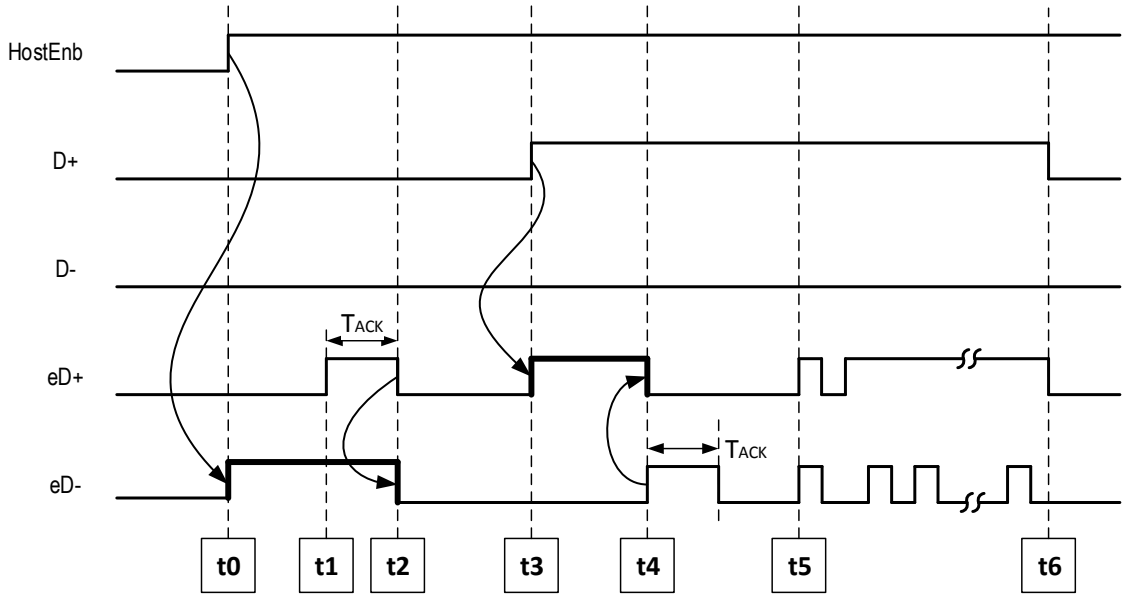


Figure 4-16: Repeater Operation upon Assertion of HostEnb (Bottom Up)

At t0, HostEnb is asserted, the repeater drives logic '1' at eD- to indicate HostEnb assertion messaging to its associate eDSPr/eUSPr.
At t1, the eUSB2 port drives an acknowledgment at eD- to acknowledge the reception of HostEnb assertion messaging.
At t2, upon detecting the conclusion of acknowledgement for HostEnb assertion messaging, the repeater concludes HostEnb assertion messaging.
At t3, upon enabling its UDSP to FS, the repeater detects USB2.0 device connect. It drives logic '1' at eD+ to signal device connect.
At t4, the host eUSB2 port transmits an acknowledgement at eD-. The repeater, upon detecting the start of the acknowledgement, concludes device connect.
At t5, the host eUSB2 issues CM.Reset.
At t6, the repeater detects CM.Reset. It switches to HS and drives USB2.0 bus reset at D+/D-.

- A eUSB2 repeater shall terminate the repeater session if one of the following conditions is met:
  - CM.Default is received under Top Down configuration. An example of a peripheral repeater terminating its repeater session is shown in Figure 4-17.
  - Either the de-assertion of HostEnb or PeripheralEnb is detected under Bottom Up configuration and a disconnect signal is transmitted. An example of host repeater terminating its repeater session is shown in Figure 4-18.
- A peripheral eUSB2 repeater shall terminate the repeater session if it has received the device disconnect announcement, or USP presence announcement. An example of device disconnect that leads to repeater session termination of a peripheral repeater is shown in Figure 4-19.
- A host eUSB2 repeater shall terminate the current repeater session if it has received DSP reset announcement, and start a new repeater session if the USB2.0 device is still connected. Note that this is a scenario, where a host eUSB2 port is under HW reset, that a new USB session needs to be started. An example of host repeater operation under DSP reset announcement is shown in Figure 4-20.

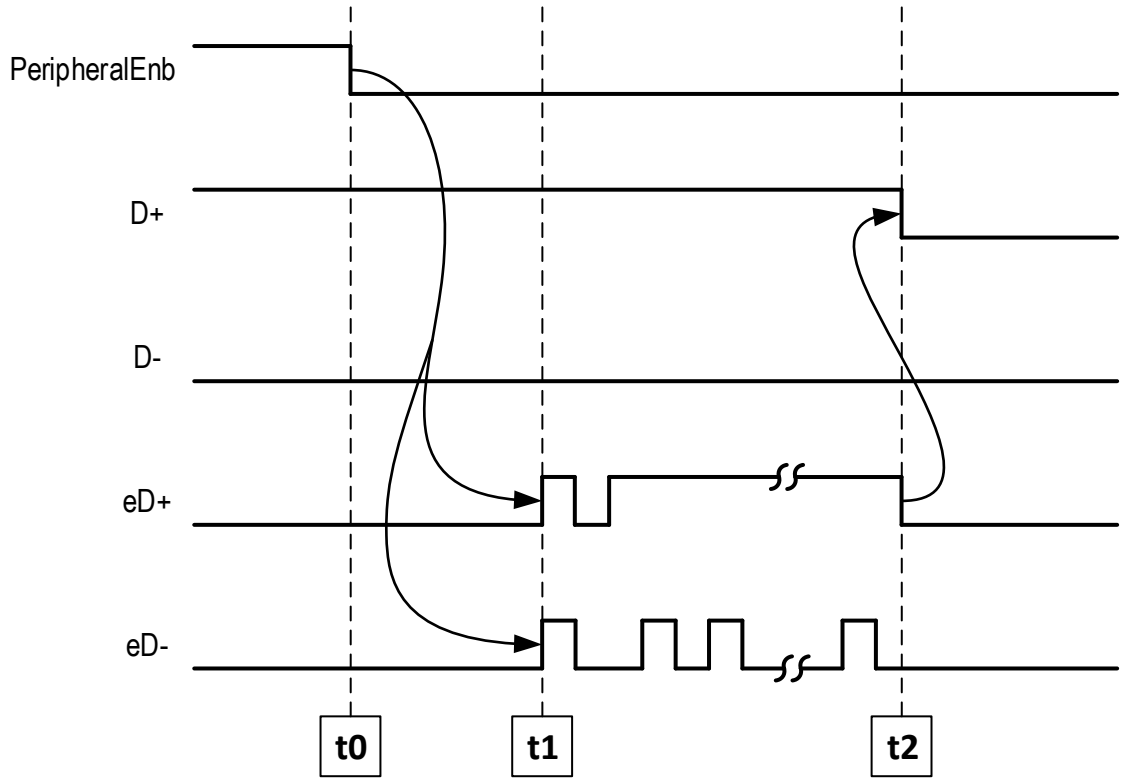


Figure 4-17: Example of a Peripheral eUSB2 Repeater Terminating Repeater Session (Top Down)

At t0, PeripheralEnb is de-asserted at the Controller. This status change is passed by the Controller to its eUSB2 port.
At t1, the eUSB2 port sends CM.Default to the Repeater.
At t2, the Repeater has received CM.Default, It turns off the pull-up resistor at D+ (or D- if this was a low speed peripheral), and resets itself to the state prior to the start of a USB session.

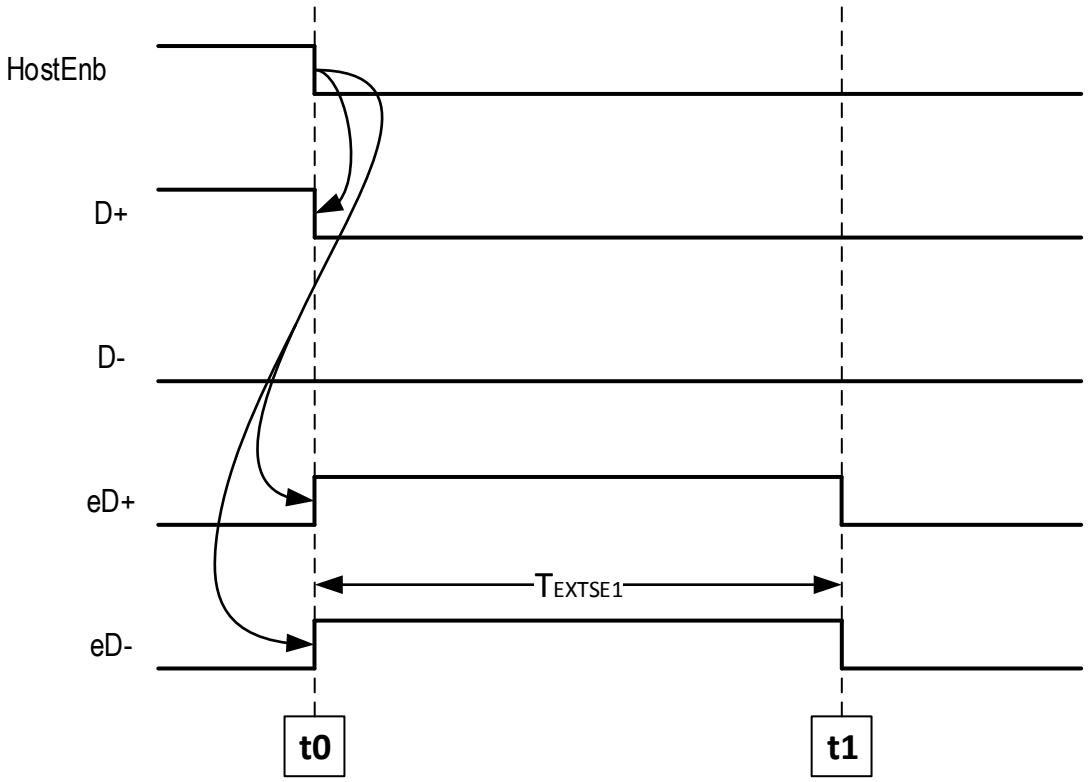


Figure 4-18: Example of Host eUSB2 Repeater Terminating Repeater Session (Bottom Up)

At t0, the eUSB2 Repeater detects de-assertion of HostEnb, it disables the transceiver at its USB2.0 port. In addition, it issues a device disconnect announcement to its associate eDSPr.

At t1, the eUSB2 Repeater concludes device disconnect announcement and returns to the Default state. Refer to Section 4.3.1 for details of repeater state machine.

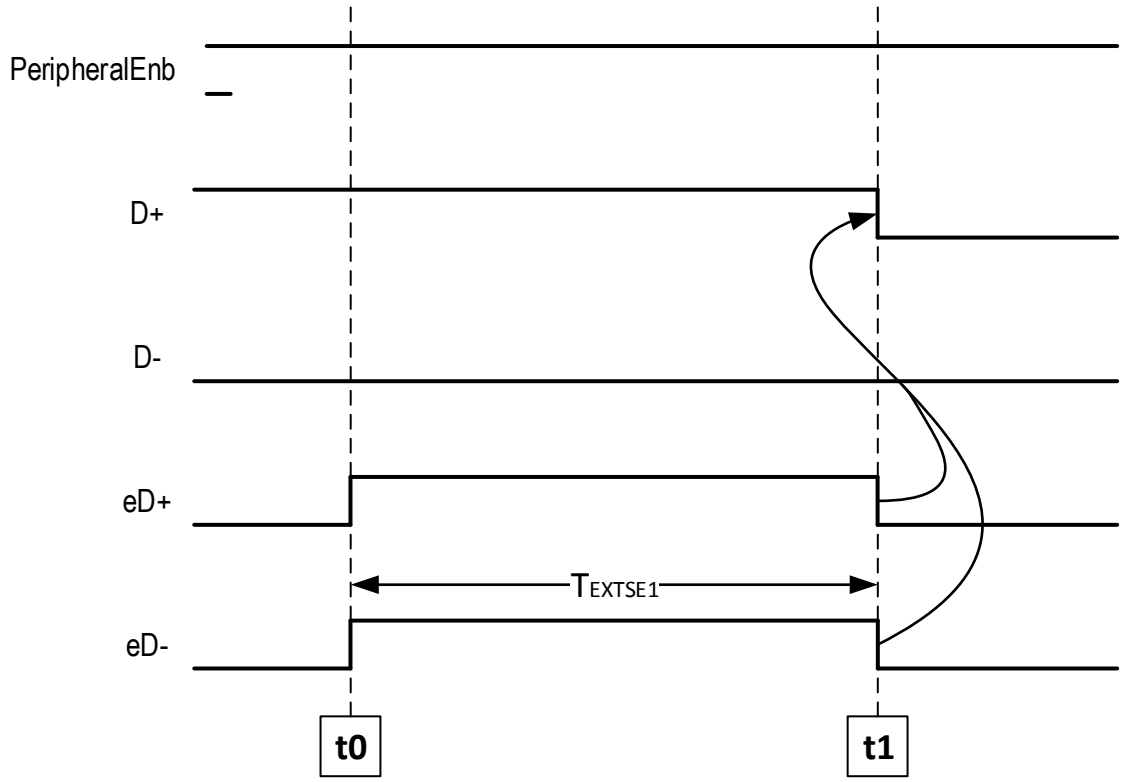


Figure 4-19: Repeater Operation upon Disconnect

At t0, Disconnect is directed by the Peripheral Controller. The command is passed to its eUSB2 port. In response, the eDSPr/eUSPr issues a device disconnect announcement to its associate repeater.

At t1, Repeater removes its pull-up resistor from D+ (or D- if it was a low speed device), and returns to the Default state. Refer to Section 4.3.1 for details of repeater state machine.

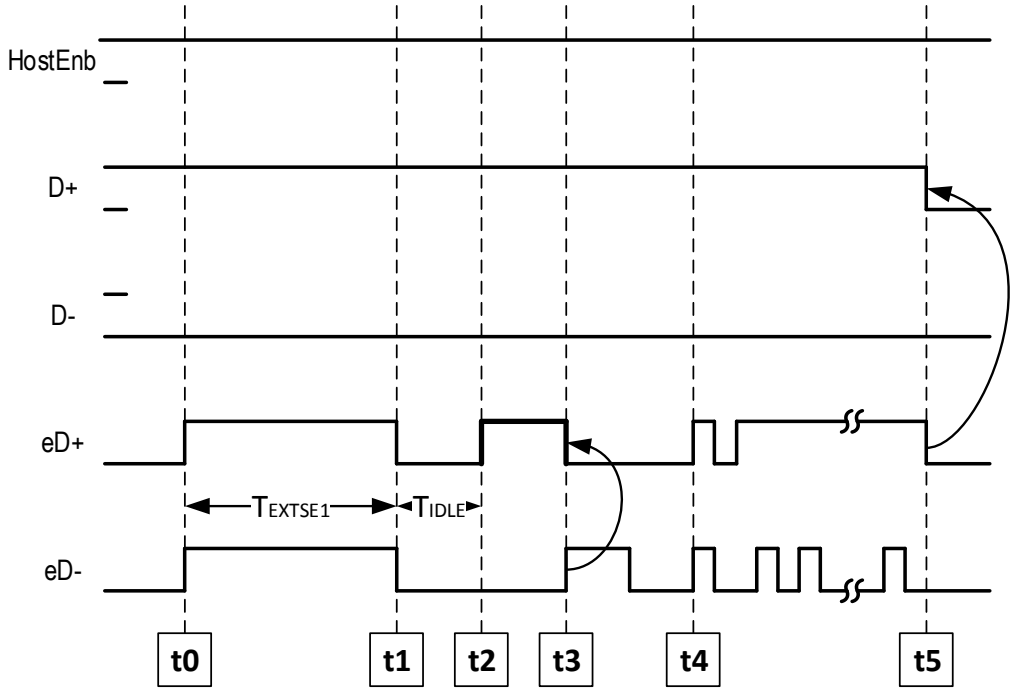


Figure 4-20: Example of Host Repeater Operation upon DSP Reset Announcement

At t0, the eUSB2 host port issues a DSP reset announcement.
At t1, the eUSB2 host repeater receives DSP reset announcement. It directs its USB2.0 port to FS.
At t2, upon observing SE0 for T_{IDLE}, the eUSB2 host repeater drives logic '1' at eD+ to replay device connect.
At t3, the eUSB2 host port acknowledges the device connect.
At t4, the eUSB2 host port issues CM.Reset.
At t5, the eUSB2 host repeater detects CM.Reset, switches to HS and drives SE0 at its USB2.0 bus.

4.3 *Repeater State Machine*

An informative two-level state machine of a eUSB2 repeater is defined. The top-level state machine defines the operation of a eUSB2 repeater from power-up to synchronization with its associate eDSPr/eUSPr in terms of TBConfig before a repeater session can be started. The second-level state machine defines the repeater operation either in the host mode or in the peripheral mode where a USB session is underway.

- The following defined repeater state machines shall apply to eUSPh, eDSPp, eUSPr and eDSPr.

4.3.1 Top Level Repeater State Machine

Shown in Figure 4-21 is the top-level repeater state machine capable of dual-role, host mode, or peripheral mode operation. Note that the state machine of a single-role repeater capable of only host mode or peripheral operation is only part of duel-role state machine where only a host mode or peripheral mode is supported. A host repeater shall only include host as its second-level state machine. A peripheral repeater shall only include peripheral as its second-level state machine.

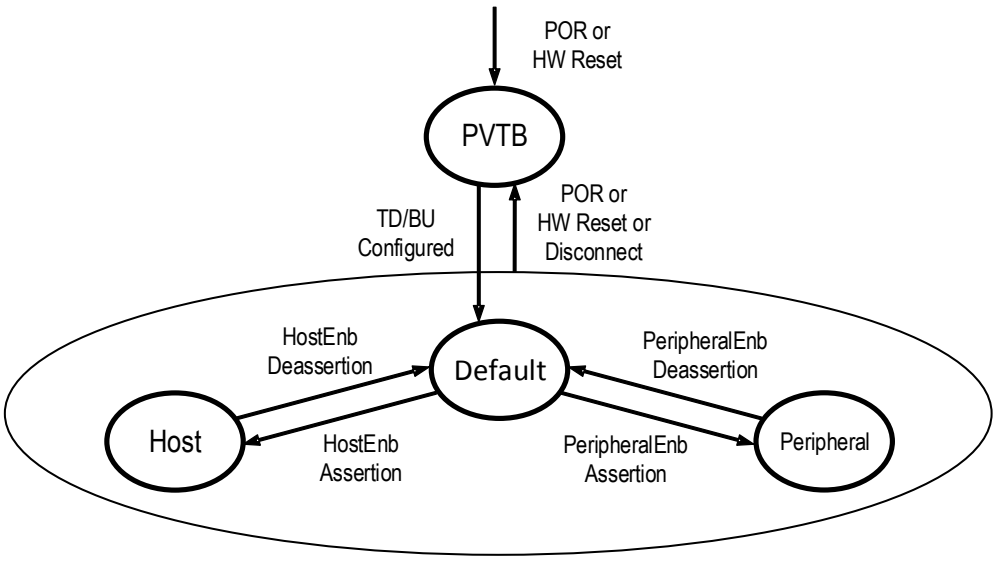


Figure 4-21: Top-Level eUSB2 State Machine

4.3.2 PVTB

PVTB is a power-on state upon POR or HW reset applied to the repeater for presence verification and TBConfig.

- A repeater shall transmit a repeater presence announcement to its associate eDSPr/eUSPr if it has observed SE0 on eUSB2 bus for T_{IDLE}.
- A repeater shall bypass repeater presence announcement if it has detected non SE0 condition on eUSB2 and perform one of the following:
    - If it is SE1, it shall monitor SE1 until its conclusion. Note that detection of SE1 upon POR may be a DSP reset announcement from a eUSB2 host port, a USP presence announcement of a eUSB2 device port or, optionally, a SCM of CM.RAP.
    - If it is non SE1, it implies a eUSB2 port has already issued a TBConfig. A eUSB2 repeater shall acknowledge TBConfig as defined in Section 4.1.3.
- A repeater and its associate eDSPr/eUSPr shall enter Default upon completing the TBConfig.

4.3.3 Default

Default is a state where the eUSB2 repeater and its associate eDSPr/eUSPr have completed mutual reset announcement and TBConfig such that a USB session may be started.

- A repeater and its associate eDSPr/eUSPr shall enter Host if HostEnb is asserted. Note that depending on the TBConfig, the propagation of HostEnb to the repeater and its associate eDSPr/eUSPr varies. Refer to Section 4.2.3 for details.
- A repeater and its associate eDSPr/eUSPr shall enter Peripheral if PeripheralEnb is asserted. Note that depending on the TBConfig, the propagation of PeripheralEnb to the repeater and its associate eDSPr/eUSPr varies. Refer to Section 4.2.5 for details.
- A repeater and its associate eDSPr/eUSPr shall enter PVTB if one of the following conditions are met.
    - POR or HW reset.
    - Received DSP reset announcement.

4.3.4 Host

Host is a state where a eUSB2 repeater and its associate eDSPr/eUSPr function as a downstream port.

- A repeater and its associate eDSPr/eUSPr shall enter Default if HostEnb is de-asserted.
- A repeater and its associate eDSPr/eUSPr shall enter PVTB upon POR or HW reset.

4.3.5 Peripheral

Peripheral is a state where a eUSB2 repeater and its associate eDSPr/eUSPr function as a downstream port.

- A repeater and its associate eDSPr/eUSPr shall enter Default if PeripheralEnb is de-asserted.
- A repeater and its associate eDSPr/eUSPr shall enter PVTB upon POR or HW reset.

4.4 *Host Repeater Operation*

This section describes basic operations of a eUSB2 host repeater associated with an eDSPr. The operation state machine of the host mode repeater is shown in Figure 4-22. The following naming conventions are used to describe the ports in operation:

- eDSP: a eUSB2 downstream port of a hub.
- eUSP: a eUSB2 upstream port of a host repeater.
- UDSP: a USB2.0 downstream port of a host repeater.

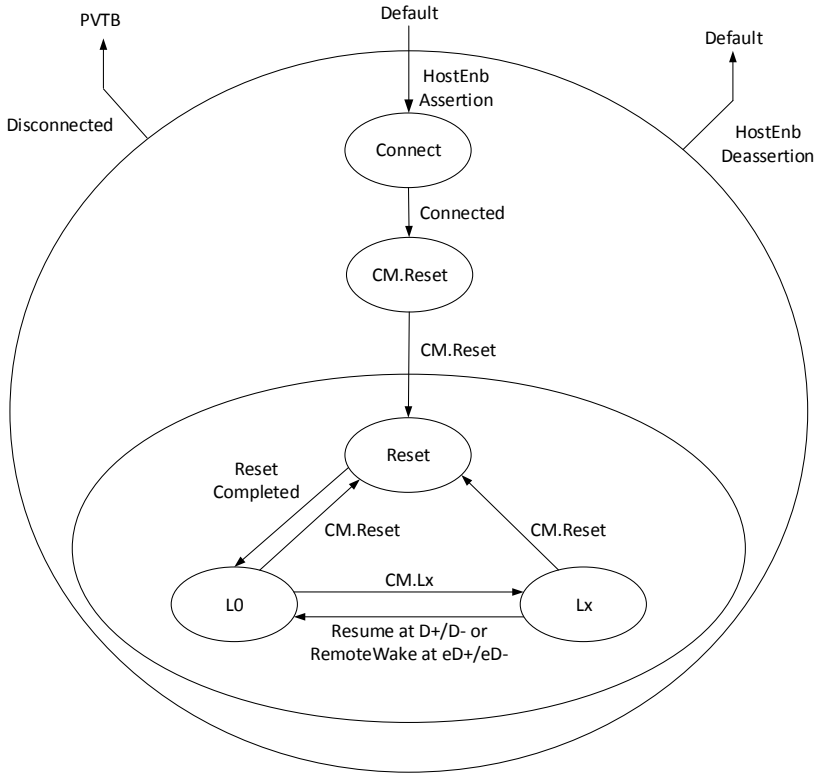


Figure 4-22: Host Mode Repeater State Machine

4.4.1 Connect

Connect is a state where the repeater operates under NREP mode. In this state, the repeater shall perform the following tasks:

- It shall enable the FS transceiver at its UDSP expecting USB2.0 device connect.
- It shall perform D+/D- debouncing for confirmation of the device connect.
- It shall be ready for control message detection.

- If it has detected the DSP reset announcement at its eDSP, it shall wait until the completion of the DSP reset announcement and prepare for device connect based on the timing defined in Section 3.6.2.5.

Connect contains two substates as shown in Figure 4-23.

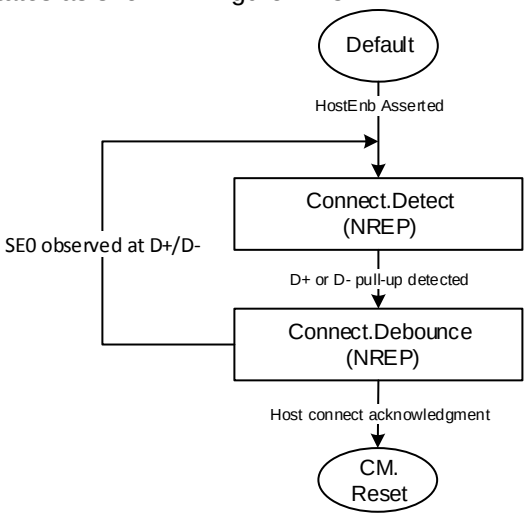


Figure 4-23: Connect Substates

4.4.1.1 Connect.Detect

Connect.Detect is a substate where the host repeater enables the FS transceiver at its UDSP in preparation for device connect.

4.4.1.1.1 Connect.Detect Requirements

- The repeater shall enable its R_{PD} at both eD+ and eD-.
- The SE receiver at its eUSP shall be enabled.
- The FS transceiver at its UDSP shall be enabled.
- The repeater shall perform USB2.0 device connect by monitoring the line state at D+/D-.
- The repeater shall remain in this substate if a DSP reset announcement is received.

4.4.1.1.2 Exit from Connect.Detect

- The repeater shall transition to Connect.Debounce if D+ or D- pull-up is detected.
- The repeater shall transition to Default if HostEnb is de-asserted.

4.4.1.2 Conect.Debounce

Connect.Debounce is a substate where the repeater relays the USB2.0 device connect event through its eUSP to eDSP until the host acknowledges device connect. The debouncing processing is performed at eDSP.

4.4.1.2.1 Connect.Debounce Requirements

The eUSP of the repeater shall meet the following conditions:

- If D+ is pulled high, it shall drive logic ‘1’ at eD+.
- If D- is pulled high, it shall drive logic ‘1’ at eD-.
- It shall drive logic ‘0’ at eD+ if it has detected the start of the host acknowledgment at eD- and disable its SE transmitter.
- It shall drive logic ‘0’ at eD- if it has detected the start of the host acknowledgment at eD+ and disable its SE transmitter.
- The repeater shall monitor until the end of the host acknowledgement.

4.4.1.2.2 Exit from Connect.Debounce

- The repeater shall transition to CM.Reset if it has detected the end of the host acknowledgment from eDSP.
- The repeater shall transition to Connect.Detect if the following two conditions are met:
    - It has detected SE0 at D+/D-.
    - It has driven logic '0' at eD+ if operating at FS/HS, or logic '0' at eD- if operating at LS.

4.4.2 CM.Reset

CM.Reset is a substate where the repeater is expecting CM.Reset.

4.4.2.1.1 CM.Reset Requirements

The eUSP of the repeater shall meet the following conditions:

- It shall keep its R_{PD} enabled.
- It shall perform SCM detection and control message decoding. Note that a repeater may also receive DSP reset announcement and shall be able to distinguish it from SCM based on its local timer.
- It shall disable it SE transmitter and enable its SE receivers upon completion of CM.Reset reception.

The UDSP of the repeater shall be in FS and continue monitoring the line state at D+/D-.

4.4.2.1.2 Exit from CM.Reset

- The repeater shall transition to Reset if the following two conditions are met:
    - It has detected SE0 at eD+/eD- after CM.Reset.
    - It has switched its transceiver to HS and driven USB2.0 bus reset at D+/D-.
- The repeater shall transition to Connect if it has detected DSP reset announcement.

4.4.3 Reset

Reset is a state where eDSP performs USB2.0 bus reset and speed detection. Reset contains multiple substates as shown in Figure 4-24.

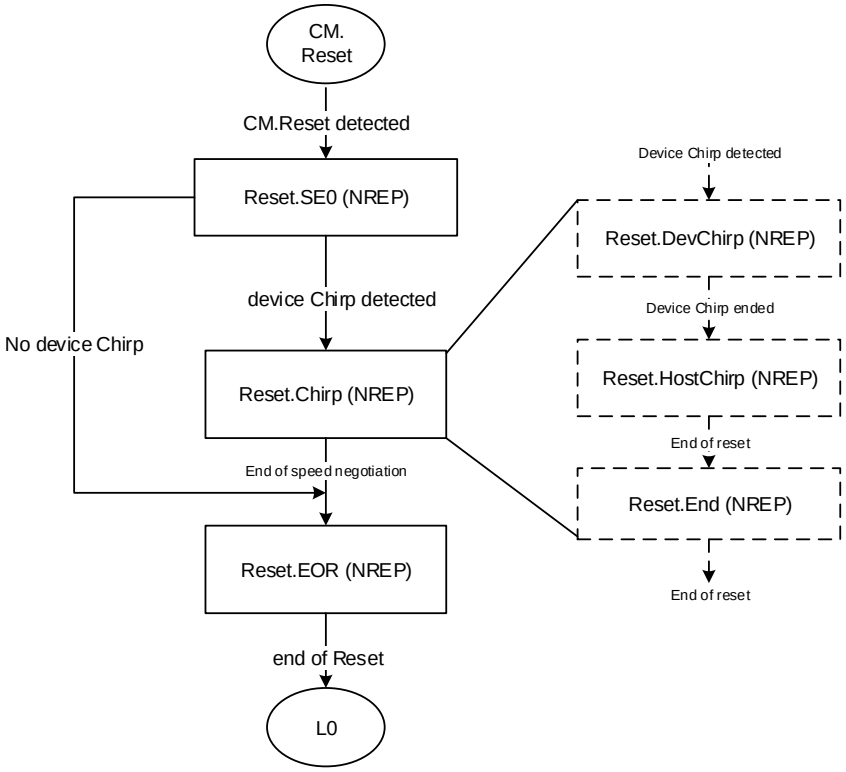


Figure 4-24: Reset Substate Machine

4.4.3.1 Reset.SE0

Reset.SE0 is a substate where the repeater is driving USB2.0 bus reset and expecting either speed negotiation or conclusion of reset.

4.4.3.1.1 Reset.SE0 Requirements

The eUSP of the repeater shall meet the following condition:

- It shall keep its SE receivers enabled.

The UDSP of the repeater shall drive USB2.0 bus reset and monitor device chirp for speed negotiation.

4.4.3.1.2 Exit from Reset.SE0

- The repeater shall transition to Reset.Chirp if device chirp is detected at UDSP.
- The repeater shall transition to Reset.EOR if it is in FS operation and has detected logic ‘1’ at eD+.
- The repeater shall transition to Reset.EOR if it is in LS operation and has detected logic ‘1’ at eD-.

4.4.3.2 Reset.Chirp

Reset.Chirp is a substate where a high-speed device is connected, and the speed negotiation is performed. There are multiple stages of operations within Reset.Chirp to complete the speed negotiation, as shown in Figure 4-24.

4.4.3.2.1 Reset.Chirp Requirements

The eUSP of the host repeater shall meet the following conditions:

- It shall enable its SE transmitter at eD+.

- It shall enable its SE receiver at eD-.
- It shall disable it high-speed transceivers and terminations during speed negotiation.

The UDSP shall meet the requirements defined by [USB2.0]. The operation of speed negotiation shall meet the following conditions. The repeater shall perform the following during device Chirp K detection, reception, and forwarding:

  - If the device Chirp K is received, it shall drive logic '1' at eD-.
  - If the device Chirp K is concluded, it shall drive logic '0' at eD- before switching to pull-down.
  - Upon completion of device Chirp K forwarding, it shall disable its SE transmitter.
- The repeater shall perform the following to forward the K-J chirps from eDSP:
  - It shall drive Chirp K at D+/D- if it has detected logic '1' at eD-.
  - It shall drive Chirp J at D+/D- if it has detected logic '0' at eD-.
  - It shall conclude K-J Chirp acknowledgment if it has detected logic '0' at eD-, and logic '1' at eD+.

4.4.3.2.2 Exit from Reset.Chirp

- The repeater shall enter Reset.EOR upon completion of K-J Chirp forwarding.

4.4.3.3 Reset.EOR

Reset.EOR is a substate where the eUSB2 host port concludes USB2.0 bus reset.

4.4.3.3.1 Reset.EOR Requirement

- If it's LS/FS operation, the repeater shall perform the eUSB2 EOR to USB2.0 EOR the same as the conversion of LS/FS eUSB2 EOP to USB2.0 EOP. Refer to Section 3.4.2.1 for details.
- If it's HS operation, the repeater shall meet the following conditions:
  - It shall drive SE0 at UDSP upon detecting rising edge of eD+.
  - It shall disable its transmitter and maintain SE0 with its R_{PD} upon detecting the falling edge of eD+, and enable its HS transceivers and squelch detectors at its eUSP and UDSP.

4.4.3.3.2 Exit from Reset.EOR

- The repeater shall enter L0 upon completing the EOR transmission.

4.4.4 L0

L0 is a state where the repeater is forwarding the USB packets between eUSB2 and USB2. L0 contains three substates as shown in Figure 4-25.

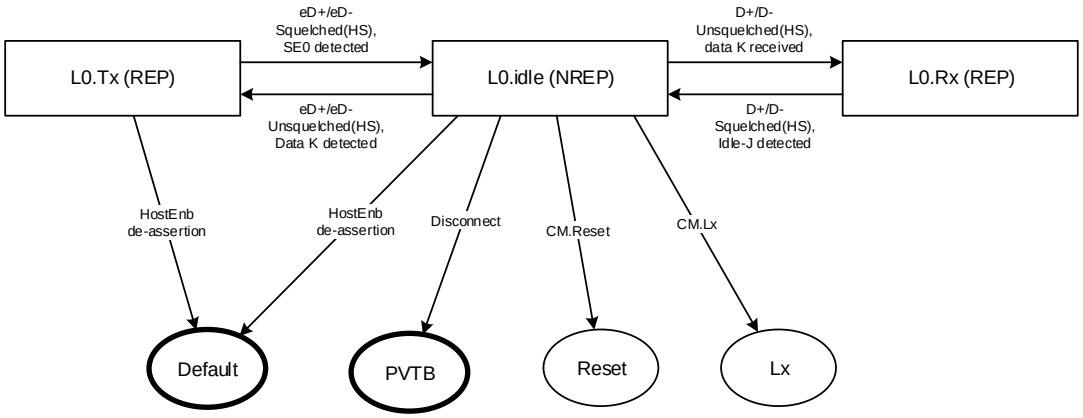


Figure 4-25: L0 Substate Machine

4.4.4.1 L0.Idle

L0.Idle is a substate where the link is idle. The repeater transitions from this substate to L0.Tx/L0.Rx based on the incoming signals from eUSP and UDSP. If it's SE1, it remains in this substate and determines if it's SCM or ESE1. If it's non SE1, it implies an incoming packet that needs to be forwarded.

4.4.4.1.1 L0.Idle Requirements

The UDSP shall meet the condition defined by [USB2.0].
The eUSP shall meet the following requirements:

- It shall enable its SE0 receivers at eD+/eD-.
- It shall enable its SE1 detector.
- If HS, it shall enable its squelch detector.

Implementation note:
Due to intra-pair skew between eD+ and eD-, a SE1, upon reaching the eUSP, may be distorted, as shown Figure 4-26.

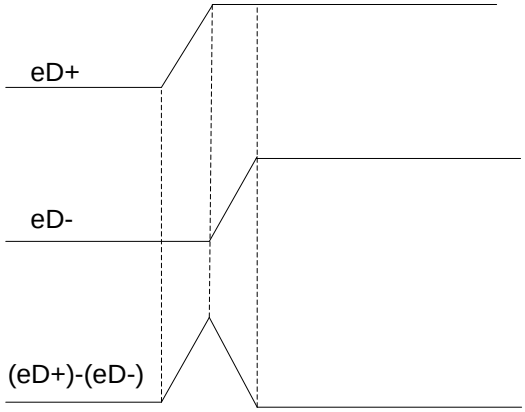


Figure 4-26: SCM Distortion Observed by eUSB2 Repeater

This distortion may exhibit one of the following false conditions to the eUSB2 repeater:

1. If the rising edge of eD+ precedes the rising edge of eD-, it may initially present itself as the first bit of SYNC in LS operation.
2. If the rising edge of eD- precedes the rising edge of eD+, it may present itself as the first bit of SYNC in FS operation, or a LS keep-alive in LS operation.
3. If either of the above two mentioned conditions occur during HS operation (L0.Idle), it may present itself as a HS K or J that may lead to HS squelch detector exiting from squelched condition.

It is highly recommended for an implementation to apply proper filtering mechanisms to avoid unintended action to those false conditions. Some possible mechanisms include the following:

1. For LS/FS operation, delayed trigger is possible since both eUSB2 and [USB2.0] allow the first bit of the SYNC pattern to be not timing compliant.
2. For HS operation, reduce the squelch detector sensitivity to not respond to the short pulse, and have the SE1 detector disable squelch detector upon declaring SE1 detection.

It is also highly desired that the eUSB2 channel construction meets the requirements defined in Table 6-6.

4.4.4.1.2 Exit from L0.Idle

- The repeater shall transition to L0.Tx if unsquelched condition is detected at eD+/eD-
- The repeater shall transition to L0.Rx if unsquelched condition is detected at D+/D-.
- The repeater shall transition to L1/L2 if CM.Lx is received at eD+/eD-.
- The repeater shall transition to Reset if CM.Reset is received at eD+/eD-.
- The repeater shall transition to Default if HostEnb is de-asserted.
- The repeater shall transition to PVTB if one of the following conditions is met:
    - A DSP reset announcement is received.
    - A device disconnect announcement is sent to eDSP upon detecting a USB2.0 device disconnect.

4.4.4.2 L0.Rx

L0.Rx is a substate where a USB packet is received and forwarded from the UDSP to the eUSP.

4.4.4.2.1 L0.Rx Requirements

- The repeater shall operate at REP mode.
- The repeater shall forward the USB packets upon detection of the unsquelched condition at the UDSP.

4.4.4.2.2 Exit from L0.Rx

- The repeater shall transition to L0.Idle upon completion of the packet forwarding detection of the squelched condition at UDSP.

4.4.4.3 L0.Tx

L0.Tx is a substate where a USB packet is received and forwarded from the eUSP to the UDSP.

4.4.4.3.1 L0.Tx Requirements

- The repeater shall operate at REP mode.
- The repeater shall enable its high-speed disconnect detector at UDSP if it operates at high-speed.

Implementation note:
High-speed disconnect detect in L0 is performed by a downstream port during EOP of SOF. It is the responsibility of the repeater to identify the EOP of an SOF. A repeater may implement a digital filter based on its local clock to detect the EOP of an SOF, and subsequently control the operation of the high-speed disconnect detector. A repeater may sample the disconnect detector output upon detection of the squelched condition at its eUSP.

4.4.4.3.2 Exit from L0.Tx

- The repeater shall transition to L0.Idle if the following conditions are met:
    - It has completed the transmission of the USB packet at its UDSP.
    - It has detected squelched condition at its eUSP.
    - It has disabled its receiver termination at its UDSP.
- The repeater shall transition to Default if HostEnb is de-asserted.
- The repeater in HS operation shall transition to PVTB if a device disconnect announcement is sent to the eDSP upon detecting USB2.0 device disconnect.

4.4.5 **Lx**

Lx is a state where the repeater is in power saving mode. The repeater power management may be different between L1 and L2, but the operation and mechanism of repeater state transition are largely the same with only the exception of device disconnect detect management. The Lx substate machine is shown in Figure 4-27.

- The repeater shall be in NREP mode.

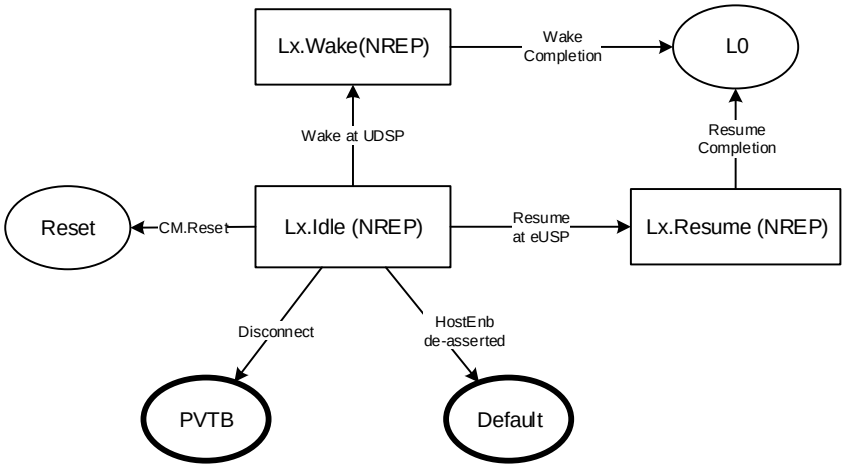


Figure 4-27: Lx Substate Machine

4.4.5.1 Lx.Idle

Lx.Idle is a substate where the repeater is in low power idle state.

4.4.5.1.1 Lx.Idle Requirements

The eUSP of the repeater shall meet the following requirements:

- It shall enable its SE receivers at eD+/eD- in expectation of SE1.
- It shall disable its high-speed transceivers.
- If the repeater enters Lx for Suspend from high-speed L0, it shall disable disconnect detect at its UDSP until CM.Detect is received. Note that contention between CM.Detect and remote wake may exist. In case it occurs, the repeater shall wait for completion of CM.Detect reception and then forward remote wake at its eUSP.

The UDSP shall meet the requirements defined by [USB2.0].

4.4.5.1.2 Exit from Lx.Idle

- The repeater shall transition to Lx.Resume if it has detected resume at the eUSP.
- The repeater shall enter Lx.Wake if it has detected remote wake at the UDSP.
- The repeater shall transition to Reset if it has received CM.Reset.
- The repeater shall transition to Default if HostEnb is de-asserted.
- The repeater shall transition to PVTB if a device disconnect announcement is sent to the eDSP upon detecting USB2.0 device disconnect.

4.4.5.2 Lx.Resume

Lx.Resume is a substate where the host starts exiting from L1 or L2.

4.4.5.2.1 Lx.Resume Requirements

- The repeater shall monitor the eUSB2 resume until its completion.
- The repeater drives the resume signal at its UDSP defined by [USB2.0] while the eUSB2 resume signal is asserted.
- If operating at LS/FS, the repeater shall transmit a LS EOP at its EDSP upon detection of the eUSB2 EOP. Refer to Section 3.4.2 for EOP transmission.

4.4.5.2.2 Exit from Lx.Resume

- The repeater shall enter L0 upon resume completion.

4.4.5.3 Lx.Wake

Lx.Wake is a substate where a [USB2.0] device initiates remote wake in order to resume the USB2.0 operation.

4.4.5.3.1 Lx.Wake Requirements

- The eUSP shall follow the eUSB2 remote wake protocol as defined in Section 3.7.2
- The UDSP shall perform the remote wake from L2 as defined by [USB2.0]. The repeater shall do the following:
  - Upon detecting remote wake at its UDSP, the repeater shall drive remote wake at its eUSP.
  - The repeater shall drive the resume signal at its UDSP from the detection of eUSB2 resume start until its conclusion.
  - The repeater shall conclude the eUSB2 remote wake signal upon detection of eUSB2 resume signal.
- The UDSP shall perform the remote wake from L1 as defined by USB2.0 Link Power Management Addendum. The repeater shall do the following:
  - Upon detecting remote wake at its UDSP, the repeater shall drive the eUSB2 remote wake at its eDSP.
  - The repeater shall drive the resume signal at its UDSP from the detection of eUSB2 resume start until its conclusion.
  - The repeater shall conclude the eUSB2 remote wake signal upon detection of eUSB2 resume signal.
- If operating at LS/FS, the repeater shall transmit a LS EOP at its UDSP.

4.4.5.3.2 Exit from Lx.Wake

- The repeater shall transition to L0 upon completion of the remote wake handshake.

4.5 *Peripheral Repeater Operation*

The state machine of a eUSB2 repeater in peripheral mode is similar to host mode but with different transition conditions. The peripheral mode repeater state machine is shown in Figure 4-28. The following naming conventions are used to describe the ports in operation:

- eUSP: a eUSB2 upstream port of a device.
- eDSP: a eUSB2 downstream port of a peripheral repeater.
  UUSP: a USB2.0 upstream port of a peripheral repeater.

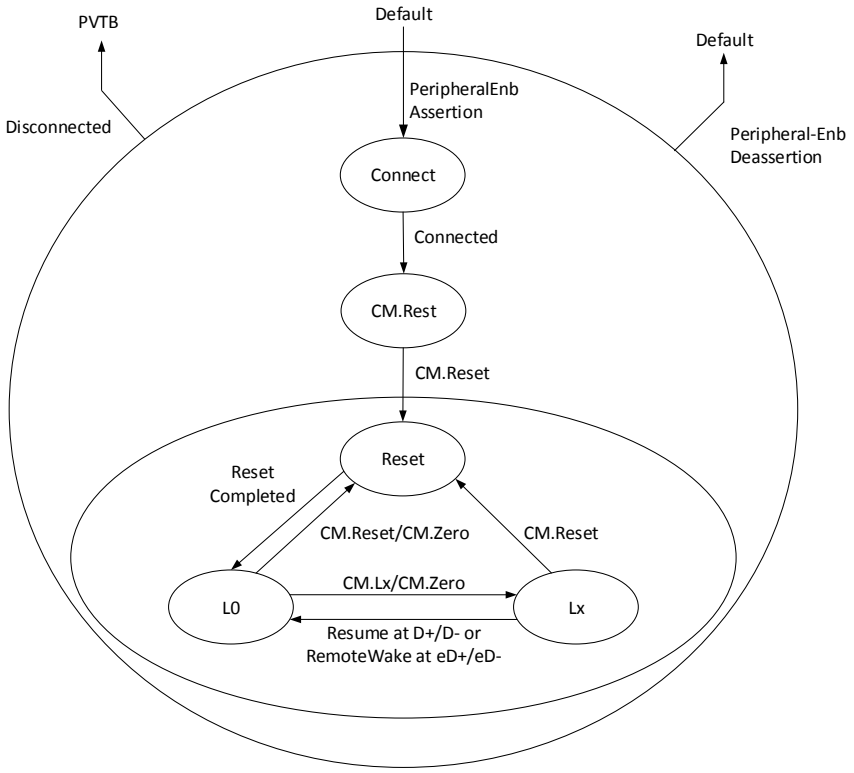


Figure 4-28: Peripheral Mode eUSB2 State Machine

4.5.1 Connect

Connect is a state where a peripheral repeater is ready for device connect directed by its controller. Connect contains two substates shown in Figure 4-29.

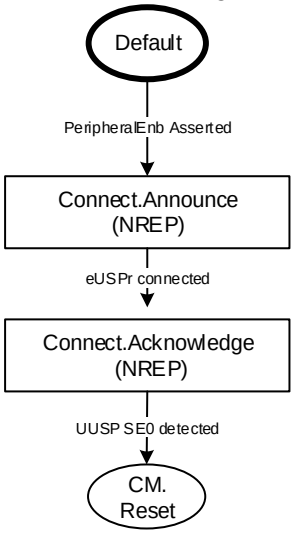


Figure 4-29: Connect Substate Machine

4.5.1.1 Connect.Announce

Connect.Announce is a substate where the eDSPp is expecting device connect from eUSPr.

4.5.1.1.1 Connect.Announce Requirements

- The eDSPp of the peripheral repeater shall meet the following conditions:

- It shall enable its R_{PD} to maintain SE0 at eUSB2 bus.
- It shall enable its SE receivers.

- The UUSP of the peripheral repeater shall have its transceivers disabled.

4.5.1.1.2 Exit from Connect.Announce

- The repeater shall transition to Connect.Acknwledge if one of the following conditions is met:
  - It has enabled FS transceiver at UUSP and pull-up at D+ upon detection logic '1' at eD+ indicating device connect for FS/HS operation.
  - It has enabled LS transceiver at UUSP and pull-up at D- upon detection logic '1' at eD- indicating device connect for LS operation.

4.5.1.2 Connect.Acknowledge

Connect.Acknowledge is a substate where the repeater is relaying device connect from its eDSPp to UUSP, and expecting host USB2.0 bus reset.

4.5.1.2.1 Connect.Acknowledge Requirements

- The eDSPp shall continue monitoring the line state at eD+/eD-.
- The UUSP shall monitor the line state at D+/D- in expecting host USB2.0 bus reset. Note that the repeater shall not sample D+/D- until D+ (FS/HS) or D- (LS) is pulled-up.

4.5.1.2.2 Exit from Connect.Acknowledge

- The repeater shall transition to CM.Reset if the following conditions are met:
  - It has detected SE0 at UUSP and started an SE0 timer.
  - It has acknowledged the device connect to the eUSPr as defined in Section 3.7.1.

4.5.2 CM.Reset

CM.Reset is a state where the peripheral repeater is qualifying SE0 at its UUSP as the USB2.0 bus reset.

4.5.2.1 CM.Reset Requirements

- The repeater shall monitor its line states at UUSP and eDSPp.

4.5.2.2 Exit from CM.Reset

- The repeater shall declare the reception of USB2.0 bus reset and transition to Reset if it has detected SE0 for more than 2.5us.

4.5.3 Reset

Reset is a state where host port performs port reset and speed detection. Reset contains multiple substates as shown in Figure 4-30.

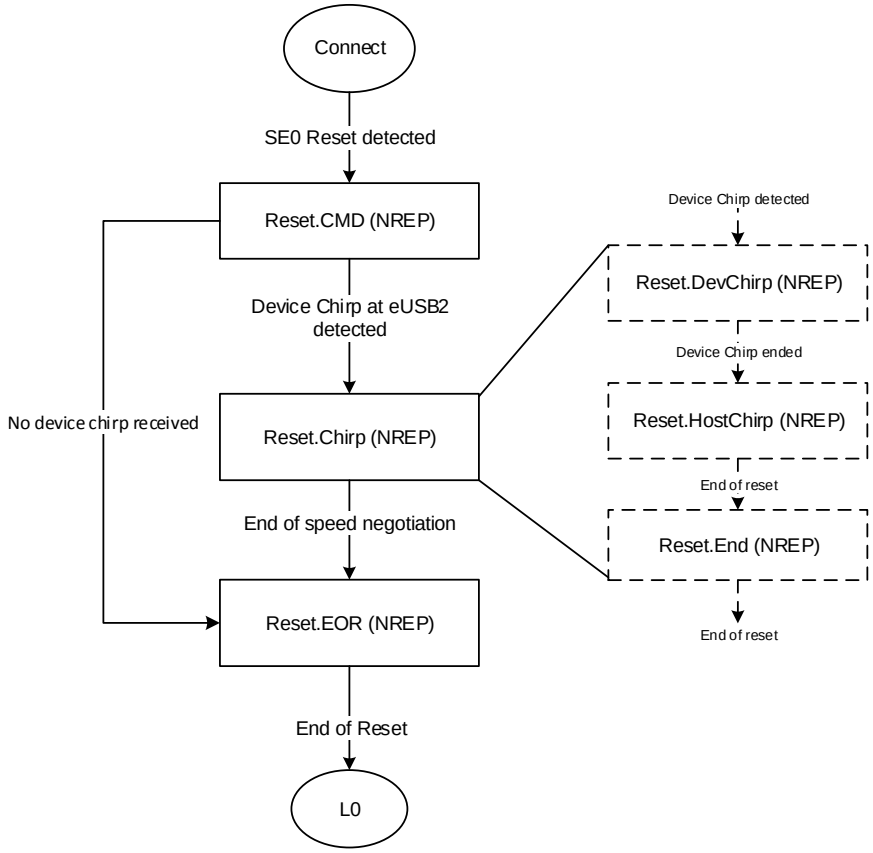


Figure 4-30: Reset Substate Machine

4.5.3.1 Reset.CMD

Reset.CMD is a substate where the repeater transmits CM.Reset and prepares for speed negotiation if its peripheral device is HS, or end of Reset if its peripheral device is LS/FS.

4.5.3.1.1 Reset.CMD Requirements

The eDSPp of the repeater shall meet the following conditions:

- It shall keep its R_{PD} at eD+/eD-.
- It shall transmit CM.Reset upon entry to this substate.
- It shall enable its SE transmitters upon completing CM.Reset transmission.
- It shall disable its SE receivers.

4.5.3.1.2 Exit from Reset.CMD

- The repeater shall transition to Reset.Chirp if device chirp is detected at its eDSPp.
- The repeater shall transition to Reset.EOR if it has detected data J at its UUSP.

4.5.3.2 Reset.Chirp

Reset.Chirp is a substate where a high-speed eUSB2 device is connected, and the speed negotiation is performed. There are multiple stages of operation within Reset.Chirp to complete the speed negotiation, as shown in Figure 4-30.

4.5.3.2.1 Reset.Chirp Requirements

- The eDSPp of the repeater shall be ready for speed negotiation by having its SE receivers enabled.

- The USB2.0 port shall enable its HS transceiver to forward device chirp K and host K-J chirp acknowledgment.
- The repeater shall forward the eUSB2 device chirp based on the following:
  - It shall drive a chirp K at D+/D- if eD- is logic '1'.
  - It shall conclude chirp K at D+/D- if eD- is logic '0'.
- The repeater shall perform the following to forward the K-J chirps from the host:
  - It shall drive logic '1' at eD- if it has detected a Chirp K at D+/D-.
  - It shall drive logic '0' at eD- if it has detected a Chirp J at D+/D-.
- It shall enable its HS receiver termination if it has detected a digital ping at eD+. Note that this is a digital ping sent by a eUSPr to inform the peripheral repeater to turn on its HS receiver termination at UUSP.
- If SE0 is detected at D+/D-, it shall conclude speed negotiation by performing the following:
  - It shall drive logic '0' at eD- and logic '1' at eD+ if it has detected SE0 at D+/D-.
  - It shall drive logic '0' at eD- and logic '1' at eD+ for T_{ACK} and then drive SE0 at eD+/eD- to conclude speed negotiation.
- Upon completion of high-speed negotiation, the repeater shall be ready for HS operation.

4.5.3.2.2 Exit from Reset.Chirp

- The repeater shall transition to Reset.EOR if SE0 is detected at UUSP.

4.5.3.3 Reset.EOR

Reset.EOR is a substate where the USB2.0 host reset is concluded. Reset.EOR does not contain any substate.

4.5.3.3.1 Reset.EOR Requirement

- The eDSPr of the repeater in LS/FS operation shall transmit an EOP defined in Section 3.4.2 to end reset based on the following:
  - If it is FS operation, it shall transmit logic '1' at eD+ for 1~2 UIs upon detection of SE0 to data J transition at D+/D-, then drive logic '0' for $T_{SE0\_DR\_LSFS}$ before concluding EOP transmission.
  - If it is LS operation, it shall transmit logic '1' at eD- for 1~2 UIs upon detection of SE0 to data J transition at D+/D-, then drive logic '0' for $T_{SE0\_DR\_LSFS}$ before concluding EOP transmission.
- If it is HS operation, it shall conclude speed negotiation and reset by performing the following:
  - It shall drive logic '0' at eD- and logic '1' at eD+ upon SE0 detection at UUSP.
  - It shall drive logic '0' at eD- and logic '1' at eD+ for T_{ACK} and then drive SE0 at eDSPr for $T_{SE0\_DR\_LSFS}$ to conclude speed negotiation and reset.
- The repeater shall enter L0 upon completion of EOP transmission.

4.5.3.3.2 Exit from Reset.EOR

- The repeater shall transition to L0 upon completing the EOP transmission at eUSB2 port.

Shown in Figure 4-31 is a timing diagram of a dual role eUSB2 peripheral repeater operation from attach to role swapping and reset/high-speed negotiation.

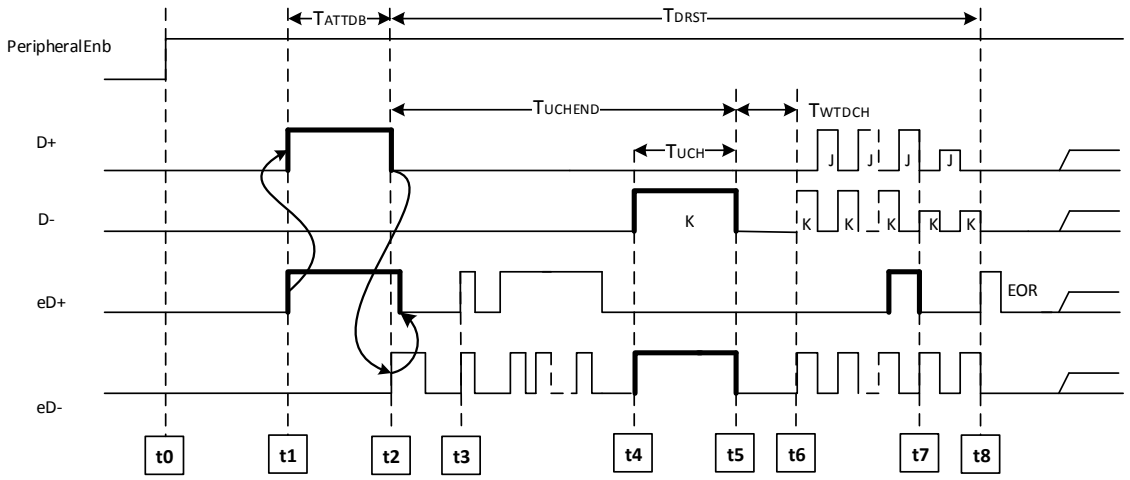


Figure 4-31: Timing Diagram of Dual Role eUSB2 Repeater from Attach to Speed Negotiation

t0. PeripheralEnb is asserted.
t1. The repeater detects logic ‘1’ at eD+, indicating a FS/HS capable eUSB2 device connect. It pulls up D+ to propagate the device connect at UUSP.
t2. The eUSB2 repeater detects SE0 on D+/D-. It drives an acknowledgment at eD-. The eUSPr, upon detecting the acknowledgment from eDSPp, drives logic ‘0’ at eD+ for $T_{SE0\_DR\_LSFS}$ to conclude connect.
t3. The repeater detects SE0 for more than 2.5uS and declares USB2.0 bus reset. It transmits CM.Reset at eD+/eD-. The peripheral eUSB2 device, upon detecting SE1, prepares its SE receivers for Control message detection.
t4. The peripheral eUSB2 device in reset drive logic ‘1’ at eD+ to indicate device chirp for T_{UCH}. The repeater drives chirp K at D+/D-.
t5. The eUSB2 peripheral device concludes device Chirp by driving logic ‘0’ at eD+. The repeater concludes chirp K accordingly.
t6. The repeater detects chirp K and J at its UUSP from the host. It forwards the host chirp by driving logic ‘1’ at eD- if chirp K is received, and logic ‘0’ if chirp J is received.
t7. After detecting the digital ping at eDSPp, the repeater turns on its HS receiver termination and is ready for HS operation. At the same time, it continues forwarding the host Chirp to the eUSB2 peripheral device.
t8. The repeater has detected SE0 or HS idle at D+/D-, indicating conclusion of host reset. It transmits an EOR at eD+ to inform the eUSB2 peripheral device the end of reset. The repeater enters L0.

4.5.4 **L0**

L0 is a state where the repeater is forwarding the USB packets between eDSPp and UUSP. Note that in peripheral mode, L0.Tx refers to packets forwarding from UUSP to eDSPp, and L0.Rx refers to packets forwarding from eDSPp to UUSP.
L0 contains three substates as shown in Figure 4-32.

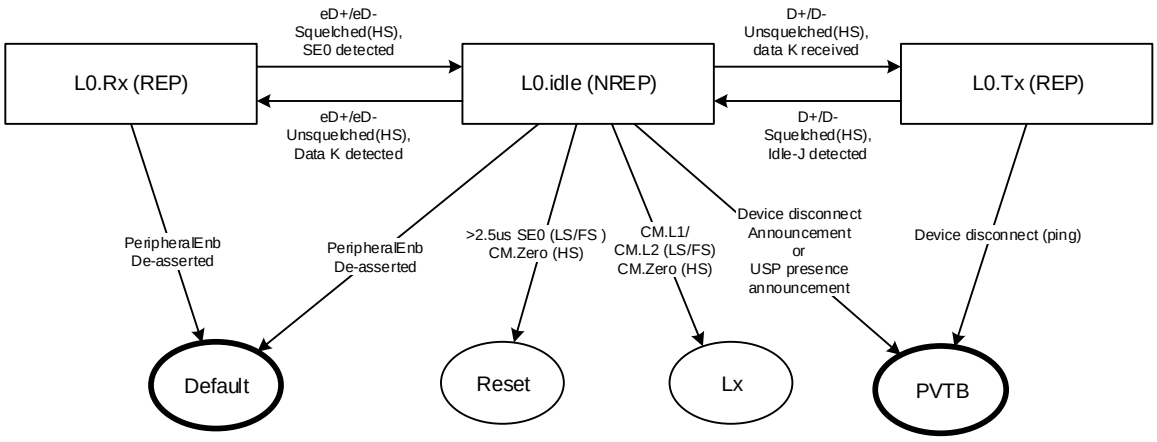


Figure 4-32: L0 Substate Machine

4.5.4.1 L0.Idle

L0.Idle is a substate where the link is idle. The repeater transitions from this substate to L0.Tx/L0.Rx based on the incoming signals from eUSB2 bus and USB2.0 bus. If it's SCM, it remains in this substate. If it's non SCM, it implies an incoming packet that needs to be forwarded.

A repeater is in peripheral mode will only receive SCM from a eUSB2 peripheral device for L1 entry.

4.5.4.1.1 L0.Idle Requirements

The UUSP shall meet the requirements defined by [USB2.0].

The eDSPp shall meet the following requirements:

- It shall enable its SE0 receivers at eD+/eD-.
- It shall enable its SE1 detector.
- If HS, it shall enable its squelch detector.
- The repeater in high-speed operation shall perform L2/reset differentiation upon receiving CM.Zero. Refer to Section 4.2.7 for details.

4.5.4.1.2 Exit from L0.Idle

- The repeater shall transition to L0.Rx if one of the following conditions is met:
  - A high-speed un-squelched condition is detected at eDSPp.
  - A LS/FS data K is detected at eDSPp.
- The repeater shall transition to L0.Tx if one of the following conditions is met:
  - A high-speed un-squelched condition is detected at UUSP.
  - A LS/FS data K is detected at UUSP.
- The repeater shall transition to Lx if the following condition is met:
  - It has received CM.L1 or CM.L2 at eDSPp.
- The repeater in high-speed operation shall transition to L2 if CM.Zero is received and the following two conditions are met:
  - It has switched to FS and observed idle J at its UUSP.
  - It has transmitted a digital ping within 50 us after receiving CM.Zero.
- The repeater in high-speed operation shall transition to reset if CM.Zero is received and SE0 at UUSP remains unchanged after switch to FS.
- The repeater in LS/FS operation shall transmit CM.Reset and transition to reset if it has detected SE0 for more than 2.5us. Note that in LS operation, a repeater may not be able to distinguish between a LS keep-alive and a reset, and transmits an extended eUSB2 LS EOP before realizing SE0 reset. Upon this condition, the

repeater shall terminate and LS EOP and transmit CM.Reset. A eUSP shall ignore the extended LS EOP.
- The repeater shall transition to Default if PeripheralEnb is de-asserted.
- The repeater shall transition to PVTB if device disconnect announcement or USP presence announcement is received.

4.5.4.2 L0.Tx
L0.Tx is a substate where a USB2.0 packet is received from UUSP and forwarded directly to the eDSPp.

4.5.4.2.1 L0.Tx Requirements
- The repeater shall operate at REP mode.
- The repeater shall forward the USB2.0 packets upon detection of a high-speed un-squelch condition or a LS/FS data K at UUSP.

4.5.4.2.2 Exit from L0.Tx
- The repeater shall transition to L0.Idle upon detection of a squelch condition at UUSP and the USB2.0 packet forwarding at eDSPp is completed.
- The repeater shall transition to PVTB if the following two conditions are met:
  - It has declared device disconnect.
  - It has disabled its transceiver at UUSP.

4.5.4.3 L0.Rx
L0.Rx is a substate where a USB2.0 packet is received from eDSPp and forwarded directly to UUSP.

4.5.4.3.1 L0.Rx Requirements
- The repeater shall operate at REP mode.
- The repeater shall forward the USB2.0 packets upon detection of a high-speed un-squelch condition or a LS/FS data K at eDSPp.

4.5.4.3.2 Exit from L0.Rx
1. The repeater shall transition to L0.Idle if the following conditions are met:
   1. It has completed the transmission of USB2.0 packet at D+/D-.
   2. It has detected a squelched condition at eD+/eD-.
2. The repeater shall transition to Default if PeripheralEnb is de-asserted.

4.5.5 Lx
Lx is a state where the repeater is in power saving mode. The repeater power management maybe different between L1 and L2, but there is no difference with respect to the operation and mechanism of repeater state transition. Lx substate machine is shown in Figure 4-33.

- The repeater shall be in NREP mode.

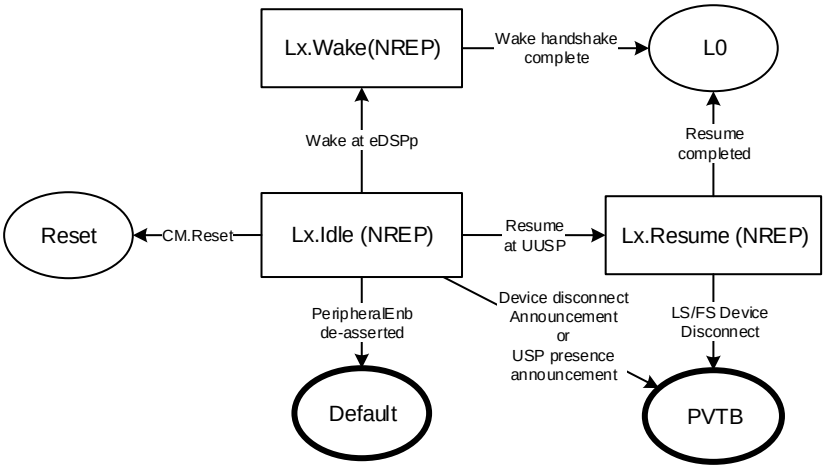


Figure 4-33: Lx Substate Machine

4.5.5.1 Lx.Idle

Lx.Idle is a substate where the repeater is in low power idle state.

4.5.5.1.1 Lx.Idle Requirements

The eUSB2 port of the repeater shall meet the following requirements:

- It shall maintain SE0 at eDSPp by enabling its R_{PD} at eD+/eD-.
- It shall enable its SE receivers at eDSPp.
- It shall disable its high-speed transceivers.

The USB2.0 port shall meet the requirements defined by [USB2.0].

4.5.5.1.2 Exit from Lx.Idle

- The repeater shall transition to Lx.Resume if it has detected resume at UUSP.
  - The repeater shall transmit CM.Reset and transition to reset if it has detected SE0 reset at UUSP If it has detected idle J to SE0 transition, and has observed SE0 for more than 2.5us.
- The repeater shall transition to Lx.Wake if it has detected remote wake at eDSPp.
- The repeater shall transition to Default if PeripheralEnb is de-asserted.
- The repeater shall transition to PVTB if it has received device disconnect announcement or USP presence announcement at eDSPp.

4.5.5.2 Lx.Resume

Lx.Resume is a substate where the host starts exiting from L1 or L2.

4.5.5.2.1 Lx.Resume Requirements

- The repeater shall drive the eUSB2 resume at eDSPp as defined in Section 3.7.2 while host is resuming.
- The repeater shall look for the digital ping from the eUSB2 peripheral device at the end of resume.

4.5.5.2.2 Exit from Lx.Resume

- The repeater shall transition to L0 upon completion of resume.
- The repeater in LS/FS operation shall declare device disconnect and transition to PVTB if it does not receive the digital ping during end of resume. Refer to Section 3.6 for details of eUSB2 device disconnect detect.

Shown in Figure 4-34 is an example timing diagram of the peripheral repeater in FS operation entering suspend and exiting on resume.

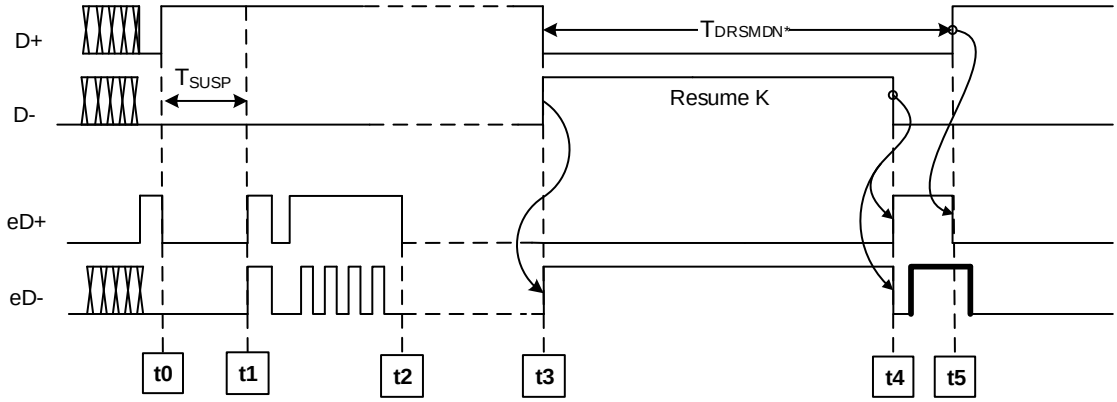


Figure 4-34: Suspend and Resume

t0. The link enters idle.
t1. Upon detecting link idle for 3ms at D+/D-, the eUSPr declares entry to suspend and transmits a CM.L2 at eD+/eD- to its peripheral repeater.
t2. Upon detecting CM.L2 at eDSPp, the repeater enters suspend.
t3. The repeater detects resume at UUSP and starts resume at its eDSPp.
t4. The repeater detects SE0 at D+/D- indicating end of resume. The repeater drives logic ‘0’ at eD-, and logic ‘1’ at eD+ indicate end of resume. The repeater detects digital ping from the eUSB2 device to indicate its presence during suspend.
t5. Upon detecting idle J at D+/D-, the repeater drives logic “0” at eD+ to end resume. The repeater enters L0 idle.

4.5.5.3 Lx.Wake

Lx.Wake is a substate where a eUSB2 peripheral device initiates remote wake to resume the USB traffic.

4.5.5.3.1 Lx.Wake Requirements

- The eDSPp shall follow the eUSB2 remote wake protocol as defined in Section 3.7.2
- The UUSP shall perform remote wake defined by [USB2.0].
- The repeater shall drive remote wake at UUSP while the remote wake signal at eDSPp is still observed. Note that the repeater in HS operation shall switch to HS driving remote wake at the UUSP, and have its HS receiver termination on.
- While driving remote wake at UUSP, the repeater shall start resume back to eUSPr.
- Upon detecting the end of remote wake at eDSPp, the repeater shall end remote at UUSP and continue to drive resume at eDSPp until the end of host resume at UUSP. Note that in an error event that no host resume is observed, a repeater may disable its UUSP, terminate resume, and issue a DSP reset announcement to start a new USB session.
- The repeater in LS/FS operation shall drive a LS EOP at the eDSPp to conclude resume.

4.5.5.3.2 Exit from Lx.Wake

- The repeater shall transition to L0 upon completion of the remote wake handshake.

Shown in Figure 4-35 is an example timing diagram of a eUSB2 repeater in peripheral mode entering suspend and exiting suspend on remote wake.

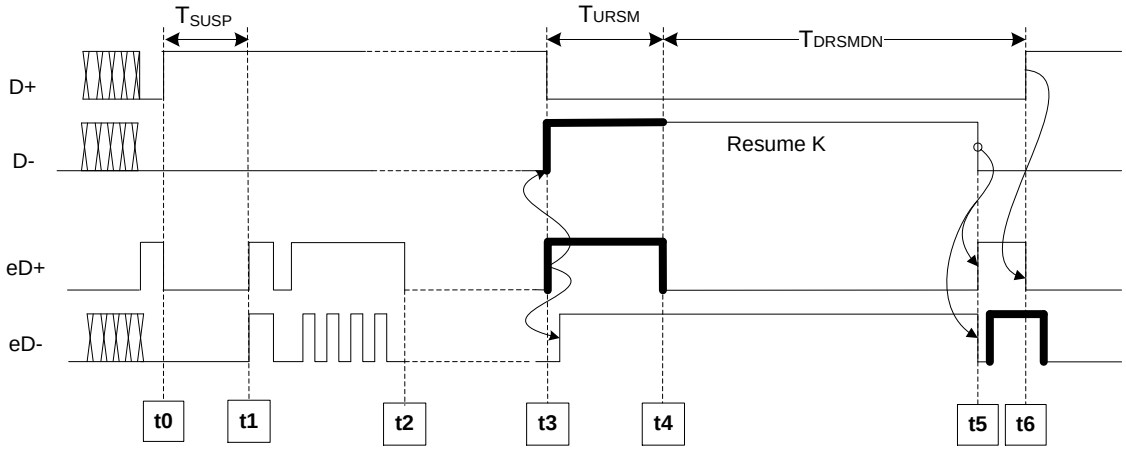


Figure 4-35: Suspend Entry and Remote Wake

t0. The link enters idle.
t1. Upon detecting link idle for 3ms, the eUSPr transmits a CM.L2 to the repeater and enters suspend.
t2. Upon detecting CM.L2, the repeater enters suspend.
t3. Upon detection of remote wake at eD+, the repeater drives remote wake at its UUSP. It also drives resume back to eUSPr at eD-.
t4. The eUSPr concludes remote wake. The repeater concludes remote wake at UUSP and continues to drive resume at eDSPp.
t5. The host USB2.0 port concludes resume with LS EOP. The repeater follows with a LS EOP at eDSPp.
t6. The repeater concludes LS EOP to end resume. It also receives digital ping from the eUSPr and enters L0.

5 Register Access Protocol

The register access protocol (RAP) is optional. It is defined for control and configuration in the following two operation modes:

- In repeater mode, for an eDSPr/eUSPr to access the register space in its associated repeater.
- In native mode, for an eDSPn to access the register space in a eUSB2 peripheral port.

The RAP bus is a point to point interconnect based on eD+ and eD-. The RAP clocking architecture is forwarded clock. The electrical requirement of the RAP is compatible with LS/FS operation defined in Chapter 6.

The RAP supports 6-bit addressing based on 2-bit command for the following byte operations:

- Read: single-byte read.
- Write: single byte write.
- Set: to perform bit-wise logic “OR” with the registered data.
- Clear: to perform bit-wise reset to the registered data with the mask.

5.1 *RAP Bus Definition and Operation*

An example RAP configuration is shown in Figure 5-1. A RAP initiator is a port initiating the register access, and it is always implemented in a eUSB2 port. A RAP receptor is a port that has

its register space implemented, and it is either implemented in a eUSB2 device, or in a eUSB2 repeater.

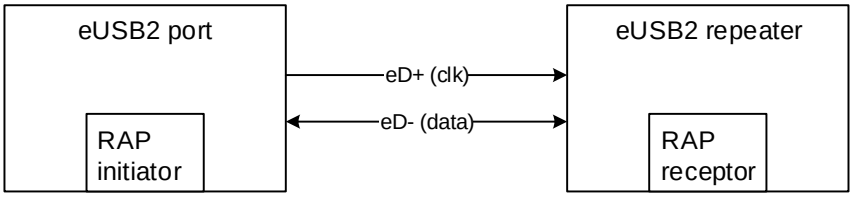


Figure 5-1: RAP Block Diagram

The RAP bus shares the eUSB2 bus. Therefore, the RAP can only be initiated when the bus is idle and no eUSB2 traffic is expected during the period of operation. The RAP may be initiated under, but not limited to the following conditions:

- Upon power up and before USB2.0 operation.
- During Suspend or L1.
- During L0 idle.

Note that it is the responsibility of the RAP initiator to manage the RAP operation without contending with the eUSB2 operation. The policy of the RAP initiation and contention avoidance is out of the scope of this document.
As shown in Figure 5-1, RAP bus is constructed based on eD+/eD-. eD+ is repurposed to carry the forwarded clock. eD- is repurposed to carry half-duplex bi-directional data. The bus clocking and operation shall meet the following requirements:

- A RAP initiator shall supply a forwarded clock to a RAP receptor for data sampling, command decoding and its associated data processing.
- The RAP bus clocking shall be based on single data rate with the RAP initiator operating on the rising edge of the clock, and the RAP receptor operating on the falling edge of the clock.
- The data bus turnaround time for data read shall be between three to sixty-four clock cycles. A RAP receptor shall first drive one cycle of logic ‘1’ and follow with the data.
- The transmission of the RAP shall start with CM.RAP and follow with the RAP command, the register address, and if the command is read, write, clear or set the data. The bit order shall be least significant bit first. Shown in Figure 5-2 is a general RAP format.
- For write operation, the RAP initiator shall drive logic ‘0’ at eD- for one clock cycle after the last bit of data (d7) is transmitted before switching to pull-down.
- For read operation, the RAP initiator shall drive logic ‘0’ at eD- for one clock cycle after the last bit of address (a5) is transmitted before switching to pull-down. The RAP receptor shall drive logic ‘0’ at eD- for one clock cycle after the last bit of data (d7) is transmitted before disabling its transmitter.
- For back to back RAP operation, the RAP initiator shall have a minimum of two cycle idle time.
- The timing of CM.RAP shall be based on $T_{CM\_UI\_Lx}$ if the link is in Lx, or $T_{CM\_UI\_L0}$ otherwise.

CM.RAP	CMD		Address						Data							
CM.16	c0	c1	a0	a1	a2	a3	a4	a5	d0	d1	d2	d3	d4	d5	d6	d7

Figure 5-2: RAP Format

5.2 *RAP Command and Features*

The RAP supports four register operation defined in Table 5-1.

Table 5-1: The RAP Command Definition

CMD (b1~0)	Operation	Description
00	Write	Data is written to the register address
01	Read	Data is read from the register address
10	Clear	Active high bit-wise clear with the data on the register address.
11	Set	Bit-wise OR with the data on the register address

An example of a write operation is shown in Figure 5-3.

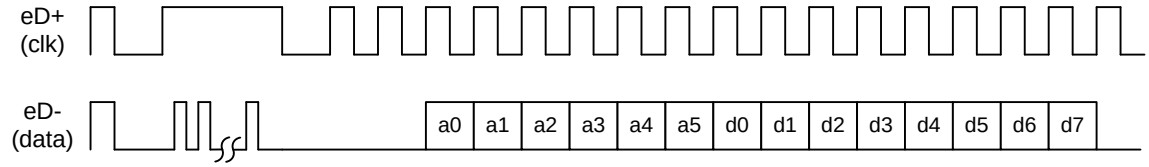


Figure 5-3: RAP Format: Write

An example of a read operation in shown in Figure 5-4.

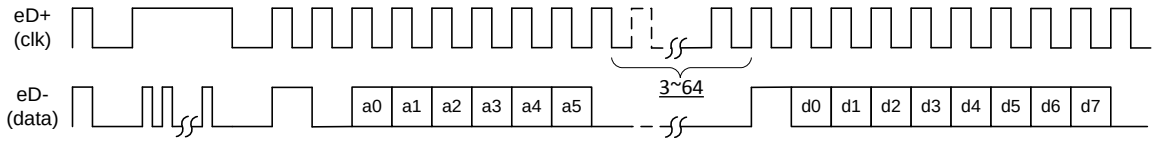


Figure 5-4: RAP Format: Read

An example of a clear operation in shown in Figure 5-5.

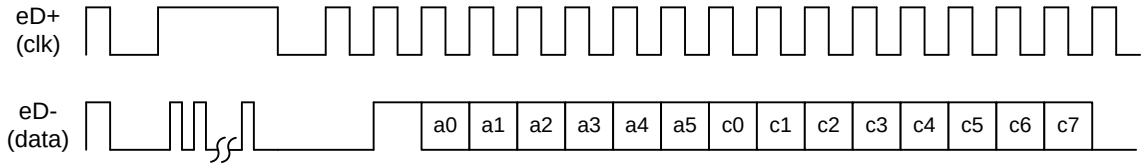


Figure 5-5: RAP Format: Clear

An example of a set operation in shown in Figure 5-6.

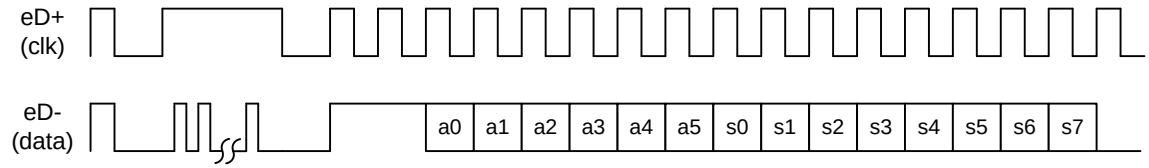


Figure 5-6: RAP Format: Set

5.3 *RAP Timing Requirement*

Shown from Figure 5-7 to Figure 5-10 are definitions of RAP timing parameters. The values of the parameters are listed in Table 5-2.

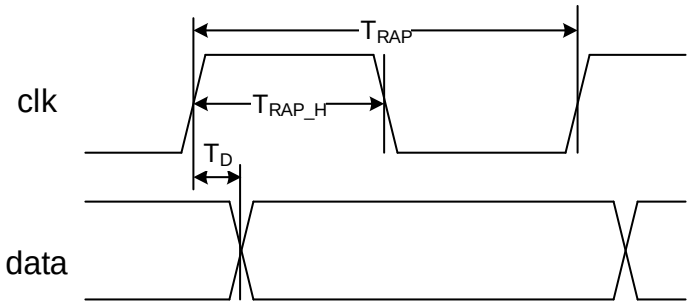


Figure 5-7: Transmitter Timing at RAP Initiator

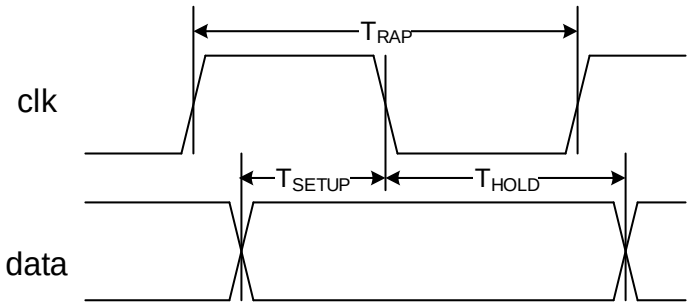


Figure 5-8: Receiver Timing at Receptor

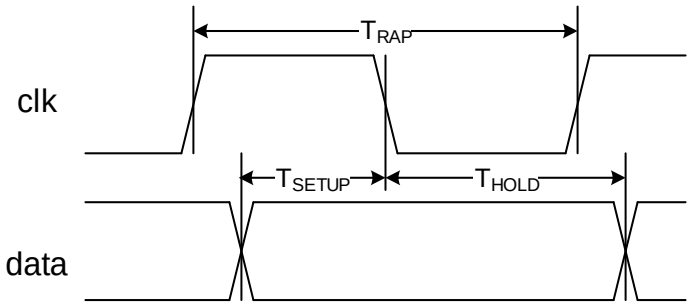


Figure 5-9: Transmitter Timing at RAP Receptor (Read Data)

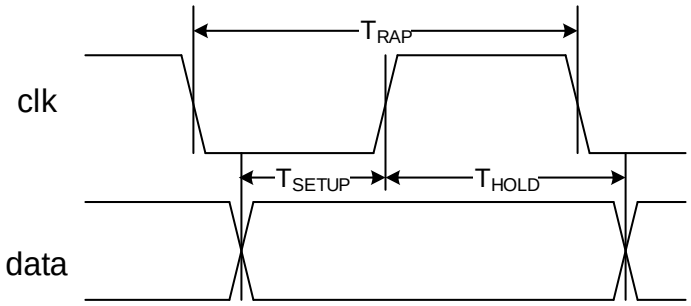


Figure 5-10: Receiver Timing at Receptor (Read Data)

Table 5-2: The RAP Timing Specification

Parameters	Min	Typical	Max	Units
T_{RAP}	166		1333	ns
T_{RAP_H} / T_{RAP}	45		55	%
T_D	0		5	ns
T_{SETUP}	25			ns
T_{HOLD}	25			ns

6 Electrical Specifications

This chapter describes the electrical specification of eUSB2.

6.1 *High-speed*

Figure 6-1 shows an example of a eUSB2 transceiver circuit. R_{SRC_HS} is the transmitter source termination. V_{TX_DIF} is the peak differential swing across the Tx eD+ and eD- pads. R_{RCV_DIF} represents the optional receiver differential termination. C_{RX_CM} is an on-die capacitor, which is recommended to suppress AC common mode fluctuation seen by the receiver. The fact that eUSB2 is a half-duplex interconnect where transmitter and receiver share the pad are omitted from the drawing in Figure 6-1.

The high-speed transceiver implements low swing differential signaling. The transmitter is required to be source terminated to deliver good signal integrity. The receiver could be differentially terminated or un-terminated. The requirement for receiver termination depends on the use case and channel characteristics. Receiver termination is a requirement for repeater mode of operation but optional for native mode.

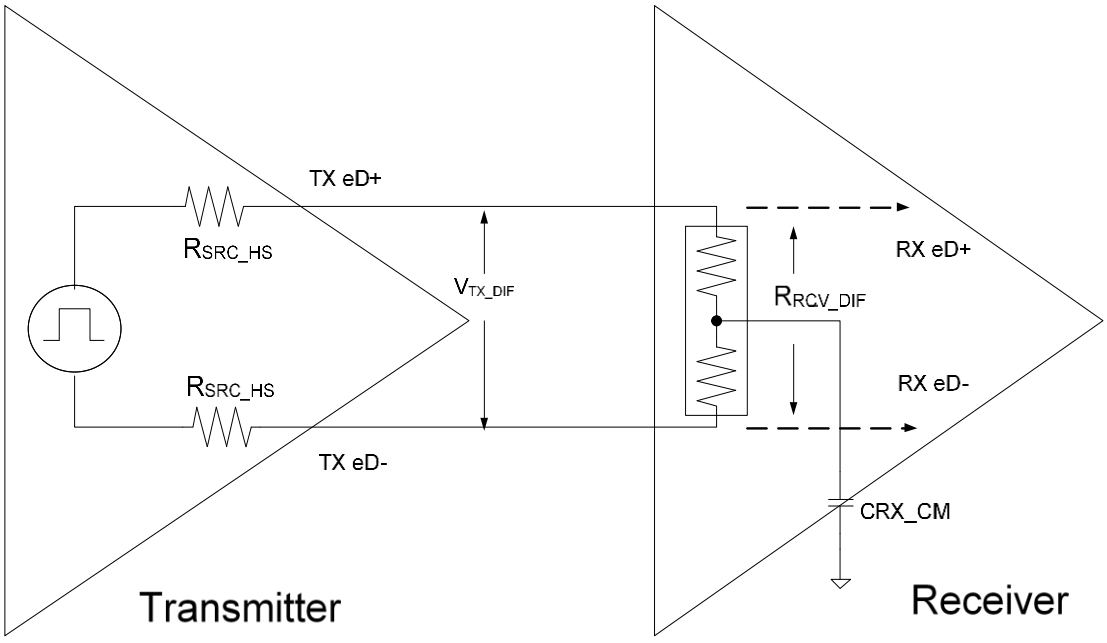


Figure 6-1: Example eUSB2 Transmitter and Receiver Circuit Structure

It is important to constrain the source impedance mismatch, ΔR_{SRC}, between Tx eD+ and eD-. The mismatch will manifest itself into common mode voltage variation which impacts both receiver functionality and system EMI performance.

The eUSB2 receiver circuit is required to extract the clock information from the incoming data stream and perform data recovery. There is no requirement to implement common clocking architecture for 2 eUSB2 devices. The clock source inaccuracy shall be less than +/- 500 ppm as defined in [USB2.0]. Spread spectrum clocking is not allowed.

The squelch circuit is implemented as an amplitude envelope detection circuit to differentiate between valid signal and wire noise. It is also used by the repeater to perform data traffic flow control. Therefore a robust squelch circuit design is critical to guarantee correct functionality.

6.1.1 High-speed Tx Electrical Specification

This section describes values at the TX pad.

Table 6-1: High-speed Transmitter DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit differential (terminated)	$V_{TX\_DIF\_TERM}$	165		245	mV	1,5
Transmit differential (un-terminated)	$V_{TX\_DIF\_UNTERM}$	360		440	mV	2,5
Transmit common mode	V_{TX_CM}	170		230	mV	3,6
Transmit source termination impedance	R_{SRC_HS}	32	40	48	Ω	6
Transmit source common mode impedance	R_{TX_CM}	16		27	Ω	6
Source impedance mismatch	ΔR_{SRC_HS}			4	Ω	4,5

Notes:

1) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-. An ideal 80Ω Rx differential termination is used as the test load.
2) The transmitter must maintain the specified differential swing after accounting for the transmit voltage supply and source termination variation at both eD+ and eD-, an 80kΩ differential termination is used as the test load.
3) The specified number does not include AC noise component.
4) The source impedance mismatch between eD+ and eD- shall not vary more than the specified max value. This impedance mismatch could result from process random variation, systematic layout offset and other sources of error.
5) The specified numbers are Informative.
6) The specified numbers are Normative.

Table 6-2: High-speed Transmitter AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit CM AC (50MHz-480MHz)	$V_{TX\_CM\_AC}$			30	+/- mV_{PEAK}	1,3

Transit rise and fall time (20%-80%)	$T_{RISE\_FALL\_TRM}$	100			ps	1,3
Transmit rise/fall mismatch				25	%	1,2

Notes:

1) Defined under an ideal 80Ω Rx differential termination with maximum supply voltage variation.
2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
3) This parameter is informative, not normative.

6.1.2 High-speed Rx Electrical Specification

Table 6-3: High-speed Receiver DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receive common mode range	V_{RX_CM}	120		280	mV	1,4
Receive center-tapped capacitance	C_{RX_CM}	15		50	pF	informative
Receive differential sensitivity	$V_{RX\_DIF\_SENS}$			60	+/- mV	4
Differential receiver termination	R_{RCV_DIF}	64	80	96	Ω	2,4
Differential receiver termination (repeater)		72	80	88	Ω	3,4
Squelch detect threshold	$V_{SQUELCH\_DIF}$	60		110	mV	4

Notes:

1) The number includes common mode variation due to Tx source impedance mismatch and 50mV ground difference between host and device. However, it does not account for receiver AC common mode variation.
2) High-speed differential receiver termination for native mode operation only
3) A tighter termination tolerance is defined for repeater mode operation to minimize accumulated jitter when propagating downstream through the repeater.
4) This parameter is normative.

Table 6-4: High-speed Receiver AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Receiver AC common mode (50MHz-480MHz)	$V_{CM\_RX\_AC}$			60	+/-mVpk	informative

6.1.3 High-speed Signal Pad Capacitance Recommendation

Table 6-5: Capacitance (Informative)

Parameter	Symbol	Min	Typ	Max	Units	Note
Tx Pad Capacitance	C_{TX}			2.5	pF	
Rx Pad Capacitance	C_{RX}			2.5	pF	

6.1.4 High-speed Channel Requirement

Native mode and repeater mode channel topologies are shown in Figure 6-2 and Figure 6-3. The informative specifications are summarized in Table 6-6.

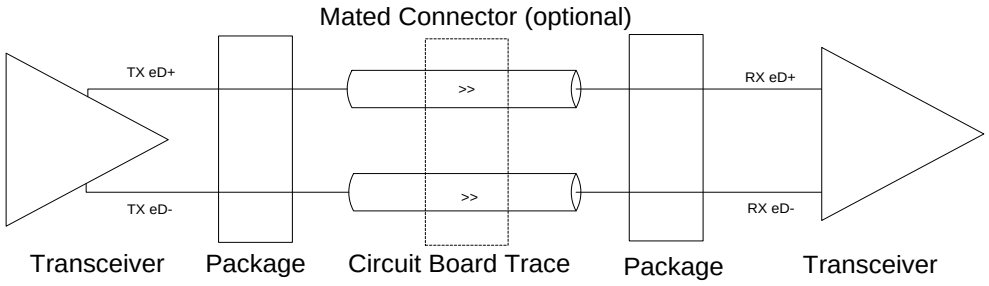


Figure 6-2: Native Mode Channel Topology

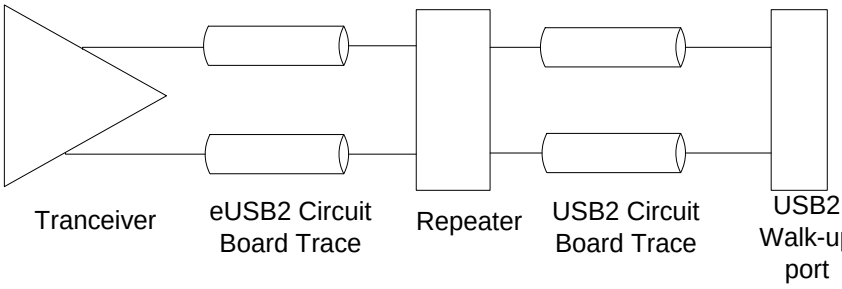


Figure 6-3: Repeater Mode Channel Topology

Table 6-6: Channel Specification (Informative)

Parameter	Symbol	Min	Typ	Max	Units	Note
Trace Differential Impedance	Z_{DIFF}		85		Ω	
Trace Differential Impedance Tolerance	ΔZ_{DIFF}			15	%	
Host-to-device insertion loss, Native Mode	IL_{NATIVE}			-1.7	dB	1,2
Host-to-repeater insertion loss, Repeater Mode	IL_{H2RPT}			-1.2	dB	1,3
Repeater-to-connector insertion loss, Repeater Mode	$IL_{RPT2CON}$			-2	dB	1,3

Notes:

1) The number is specified at 240MHz frequency.
2) Refer to Figure 6-2 for the topology setup.
3) Refer to Figure 6-3 for the topology setup.

6.1.5 High-speed Eye Diagram and Jitter Allocation

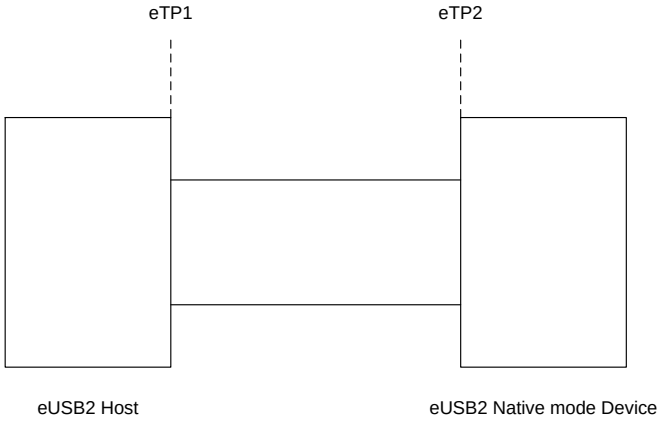


Figure 6-4: Measurement Plane for Native Mode

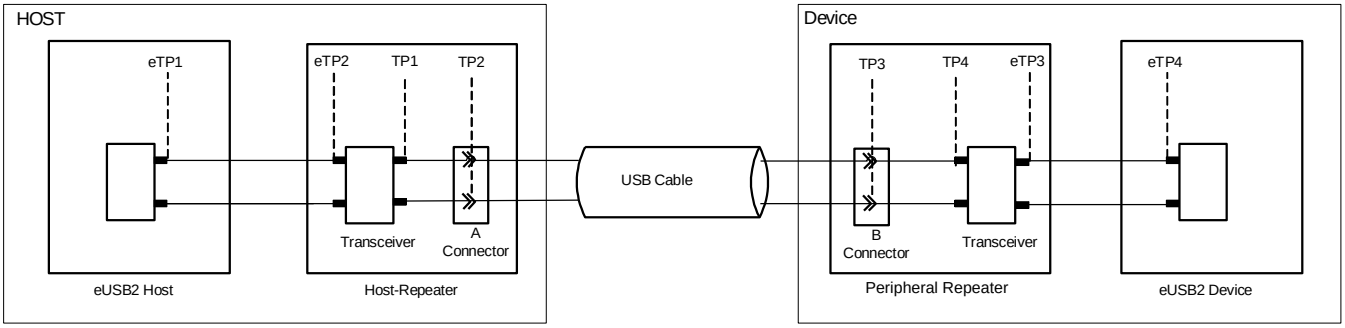


Figure 6-5: Measurement Plane for Repeater Mode

Figure 6-6 defines 4 additional test planes[1] eTP1, eTP2, eTP3 & eTP4. Definition of TP2 and TP3 remains the same as specified by [USB2.0], section 7.1.2.2.

- eTP1 and eTP2 are the points where the IC pins of the eUSB2 Host and eUSB2 host repeater are respectively soldered to the circuit board.
- eTP3 and eTP4 are the points where the IC pins of eUSB2 Repeater and eUSB2 Device are respectively soldered to the circuit board.

Two additional templates have been defined by the eUSB2 specification. eUSB2 jitter budgeting assumes jitter at TP2 & TP3 remain the same as defined in [USB2.0]. USB2.0 Template1 & Template 4 are normative specifications. eUSB2 Template 1 & eUSB2 Template 2 are informative specifications only during repeater mode. Conformance to eUSB2 Template 1 and 2 is required for eUSB2 Host and eUSB2 device in native mode.

eUSB2 Template 1: Transmit waveform requirement for a eUSB2 host measured at eTP1.
eUSB2 Template 2: Receiver sensitivity requirements for a eUSB2 device when signal is applied at eTP2 (native mode) or eTP4 (repeater mode).

Note1: eUSB2 templates have been defined assuming signal flow where eUSB2 Host in transmit mode is transmitting to eUSB2 device in receive mode. Host repeater's eUSPh is in receiving

mode & D+/D- side in transmit mode while Peripheral repeater's eDSPp is in transmit mode & D+/D- side is in receiving mode. Jitter allocation for a repeater is 50ps.

6.1.5.1 eUSB2 Template 1

Figure 6-6 defines the setup for the simulation/measurement. The circuit board trace should be kept less than one inch, and R_L differential termination resistor should be 80kΩ+/- 1% for unterminated mode and 80Ω +/- 1% for terminated mode.

Figure 6-7 shows the transmit waveform requirement for a eUSB2 host measured at eTP1. It should be read together with Table 6-7 or Table 6-11 depending on the application. Table 6-8 and Table 6-9 define V-T limits for un-terminated and terminated load respectively.

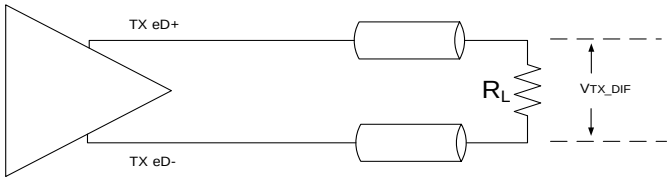


Figure 6-6: High-speed Transmit Eye Diagram Test Setup

Table 6-7: High-speed Transmit Eye Test Load Definition

Termination	R_L
Terminated	80Ω
Unterminated	80kΩ

Note: for measurement at pin.

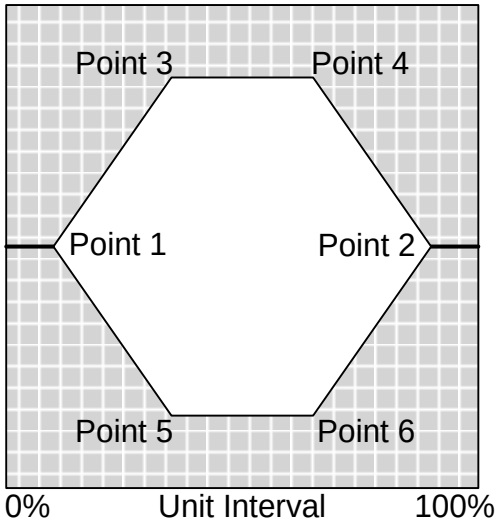


Figure 6-7: eUSB2 Template 1 Eye Mask

Table 6-8: eUSB2 Template 1 V-T Table (Un-terminated)

	80kΩ test load	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	10
Point 2	0V	90
Point 3	180mV	35
Point 4	180mV	65
Point 5	-180mV	35
Point 6	-180mV	65

Table 6-9: eUSB2 Template 1 V-T Table (Terminated)

	80Ω test load	
	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	4
Point 2	0V	96
Point 3	150mV	35
Point 4	150mV	65
Point 5	-150mV	35
Point 6	-150mV	65

6.1.5.2 eUSB2 Template 2

Receiver eye patterns specify the minimum and maximum limits, as well as limits on timing jitter, measured at the 80**Ω** differential test load at the end of the channel. Figure 6-8 shows the Receiver sensitivity requirements for a eUSB2 device when signal is applied at eTP2 (Native mode), and for a eUSB2 device with repeater when signal is applied at eTP4. Table 6-10 defines the V-T limits of the eye mask.

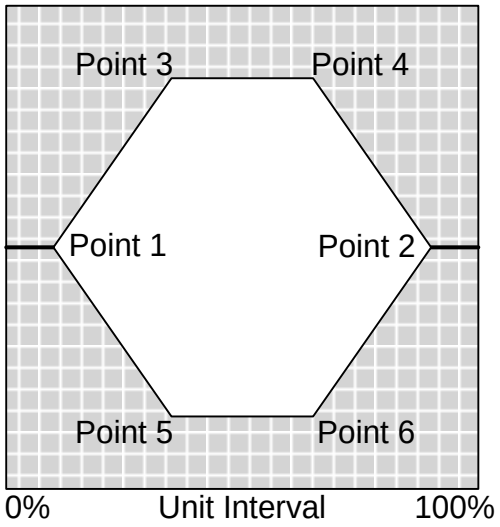


Figure 6-8: eUSB2 Template 2 Eye Mask

Table 6-10: eUSB2 Template 2 V-T Table

	Voltage Level (eD+ - eD-)	Time (% of UI)
Point 1	0V	21.2
Point 2	0V	79.8
Point 3	110mV	41.2
Point 4	110mV	58.8
Point 5	-110mV	41.2
Point 6	-110mV	58.8

6.1.5.3 High-speed Repeater Mode Jitter Allocation

USB2 Tx and Rx Eye Diagram compliance requirements dictate the total jitter allocation available to the transmitter, repeater and the channel.

A redriver is recommended if the channel topology between the SoC and walk-up port is meeting the specification outlined in section 6.1.4. For applications that require channel route beyond the specification, a retimer is required.

A redriver is required to comply with Template 1 (in the case of host repeater) & Template 4 (in the case of peripheral repeater) as defined in [USB2.0], Section 6.1.2.2, when repeater signals either to upstream or downstream. A detailed system level Jitter Budget is given in Table 6-11. The baseline for this jitter budget is maintaining the same jitter budget as TP2 & TP4 as defined in USB2.0 Template 1 & Template 4. Note that this requirement does not apply to a retimer. A retimer should be treated like a typical USB2.0 hub from jitter budgeting perspective.

Table 6-11: System Level Jitter Budgeting with Host & Peripheral Redriver

Jitter Source	Tj (ps)	UI (%)	Note
eUSB2 Tx	166.5	8	1
Host Channel	96	4.6	2
Host-Redriver	50	2.4	3
USB Cable	312.5	15	
Device Channel	208.3	10	2
Peripheral Redriver	50	2.4	3
Total	883.3	42.4	4,6

Notes:

1. Silicon TX jitter budget is informative.
2. Channel jitter is informative.
3. Repeater jitter is normative and measured during test mode using Test Packet.
4. Total jitter at eTP4 is informative.
5. Total jitter at TP2 & TP3 is normative and complies with USB2.0 Template 1 & Template 3 as defined in [USB2.0].
6. Receiver must tolerate an additional 2.4% jitter.

6.2 *Low-speed/Full-speed*

[JESD8-14A.01] Normal Range Voltage Supply standard forms the basis for Low-speed/Full-speed DC electrical specification.

Low-speed/Full-speed used single-ended CMOS signaling to communicate between the link partners. A relatively loose source termination is required if compared to High-speed. The receiver is un-terminated. Limits are defined for rise and fall time to avoid excessive overshoot and undershoot observed at both the transmitter and receiver end.

6.2.1 Full-speed/Low-speed Electrical Specification

Table 6-12: Low-speed /Full-speed DC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit single-ended output low	V_{OL}			0.275	V	1
Transmit single-ended output high	V_{OH}	0.675			V	1
Transmit output impedance	R_{SRC_LSFS}	55		120	Ω	2
Input low voltage	V_{IL}	-0.2		0.38	V	1
Input high voltage	V_{IH}	0.58		1.3	V	1
Receive single-ended hysteresis voltage	V_{HYS}	50			mV	1,2

Notes:

1) Specification defined with reference to [JESD8-14A.01] normal operating range.
2) Must be met up to V_{OL} when driving low and above V_{OH} when driving high.

Table 6-13: Low-speed /Full-speed AC Specifications

Parameter	Symbol	Min	Typ	Max	Units	Notes
Transmit rise and fall time (10%-90%)	$T_{RISE\_FALL\_TRM}$	0.8		10	ns	1
Transmit rise/fall mismatch				25	%	2

Notes:
1) Measured with 2.5pF test load at eUSB2 device/eUSB2 repeater end and assuming 10 inch channel trace in between eUSB2 Host and eUSB2 repeater/eUSB2 device.
2) Rise/fall mismatch = absolute delta of (rise – fall time) / (average of rise and fall time).
3) To get better system performance try to match termination impedance as close as possible

6.3 *Pull-down*

A much stronger pull-down is defined for eUSB2. Pull-downs are used during device connect detect. It is also used to hold the line to ground when the link is idle.

Table 6-14: Host and Device Pull-up and Pull-down Specification

Parameter	Symbol	Min	Typ	Max	Units	Notes
Pull-down	R_{PD}	4		10	kΩ	

6.4 *Timing Specification*

Table 6-15: Timing Specification

Parameter	Symbol	Min	Typ	Max	Units	Notes
The amount of time that an active driver shall continue to drive the wire to transition from non-SE0 to SE0, before letting the weak pull-down to hold the wire in SE0 idle, for low-speed and full-speed mode.	$T_{SE0\_DR\_LSFS}$	20		70	ns	
The amount of time that an active driver shall release driving SE0 from non-SE0 to SE0, before letting the weak pull-down hold the wire in SE0 idle.	$T_{SE0\_DR\_HS}$	20		70	ns	The min and max are determined by the allowable clock ppm.
Valid TBConfig	$T_{TBConfig}$	0.5			us	

Parameter	Symbol	Min	Typ	Max	Units	Notes
Start of Control Message during L0	$T_{CM\_SE1\_L0}$	0.5		2.5	us	
Control message unit interval during L0	$T_{CM\_UI\_L0}$	0.5		2.5	us	
Start of Control during L1/L2	$T_{CM\_SE1\_Lx}$	5		25	us	
Control message unit interval during Lx	$T_{CM\_UI\_Lx}$	5		25	us	
SE0 idle duration after SE1 detection	T_{IDLE}	100			us	
Time duration of the extended SE1	T_{EXTSE1}	30		50	ms	
Time duration of DSP reset announcement	$T_{SE1\_DSPReset}$	30		50	ms	
Time from internal power good to device pulling D+/D- beyond VIHZ (min) (signaling attach)	T_{SIGATT}			100	ms	[USB2.0]
Debounce interval provided by USB system software after attach	T_{ATTDB}			100	ms	[USB2.0]
Duration of an acknowledge signal from host after the device has signaled connect by driving eD+/eD- to logic “1”	T_{ACK}			5	us	Event driven. Must be driven until eD+ goes low.
Duration of driving reset to a downstream facing port	T_{DRST}	10		20	ms	[USB2.0]
Reset Recovery Time	T_{RSTRCY}			10	ms	[USB2.0]
Duration of driving WakeOnEvent pin HIGH from repeater to SoC	$T_{WakeOnEvent}$	1		10	ms	
From downstream Resume Timing to the time a digital ping is asserted by a device during L2 resume	$T_{RSM\_ACK\_START}$			16	ms	

Parameter	Symbol	Min	Typ	Max	Units	Notes
From downstream Resume Timing to the time a digital ping is de-asserted by a device during L2 resume	$T_{RSM\_ACK\_END}$			18	ms	
Period of L0 Idle before Single-ended disconnect signaling	T_{DRHDD}	4			ms	
Duration of driving resume to a downstream port; only from a controlling hub	T_{DRSMDN}	20			ms	[USB2.0]
Period of idle bus before device can initiate resume	T_{WTRSM}	5			ms	[USB2.0]
Duration of driving resume upstream	T_{DRSMUP}	1		15	ms	[USB2.0]
Time from detecting downstream resume to rebroadcast	T_{URSM}			1	ms	[USB2.0]
From downstream Resume Timing to the time a digital ping is asserted by a device during L1 resume	$T_{L1RSM\_ACK\_START}$			5	us	
From downstream Resume Timing to the time a digital ping is de-asserted by a device during L1 resume	$T_{L1RSM\_ACK\_END}$			6	us	
Time duration from entry to L1 to start of disconnect detection	$T_{L1DiscRec}$	50		250	us	
Time duration from entry to suspend to start of disconnect detect	$T_{L2DiscRec}$	3		4	ms	[UTMI+ v1.0]
L1 Residency	$T_{L1Residency}$	50		>50	us	LPM Addendum
Host initiated L1 Exit Host drives resume time	$T_{L1HubDrvResume1}$	50±1		1200±1	us	LPM Addendum
Host/Hub drive resume in response to Device remote wake	$T_{L1HubDrvResume2}$	60±1		990±1	us	LPM Addendum
Device initiated L1 Exit Device drives resume time	$T_{L1DevDrvResume}$	50±1			us	LPM Addendum

Parameter	Symbol	Min	Typ	Max	Units	Notes
Host/Hub detect and begin reflecting resume	$T_{L1HubReflect}$			48	us	LPM Addendum
Time from internal power good to driving logic “1” at eD+/eD-	T_{SIGB}			50	ms	
Minimum duration of a Chirp K from a high-speed capable device within the reset protocol	T_{UCH}	1			ms	USB2.0
Time after start of SE0 by which a high-speed capable device is required to have completed its Chirp K within the reset protocol	T_{UCHEND}			7	ms	USB2.0
Time after end of device Chirp K by which hub must start driving first Chirp K in the hub’s chirp sequence	T_{WTDCH}			100	us	USB2.0
From micro-B unplug to repeater signal host disconnect signal to SoC Dual Role Port	T_{HDIS}			20	ms	
Time after a micro-B unplug event is detected to SoC Dual Role Port resumes host role	T_{ROLE_RESUME}			20	ms	
Digital ping response delay	T_{PING_LSFS}	20		50	ns	
Width of the analog ping during L0 idle for device presence indication	$T_{PING\_W\_HS}$	40		100	ns	
Transmit delay of the analog ping	$T_{PING\_D\_HS}$			40	ns	
Differential Skew (at Rx)	T_{SE1_SKEW}			500	ps	Measured at 50% cross-over point
Digital Ping pulse width during resume	$T_{PING\_HS\_RDY}$	100		500	ns	

Note: If there is a discrepancy between the numbers in the eUSB2 specification and the core specification, use the core specification numbers.

Appendix A Skew and Rise/Fall time Break-ups

The skew and rise/fall time break-up for T_{SE_SKEW} can be found below. Refer to Figure A-1 for skew sources in the communication channel.

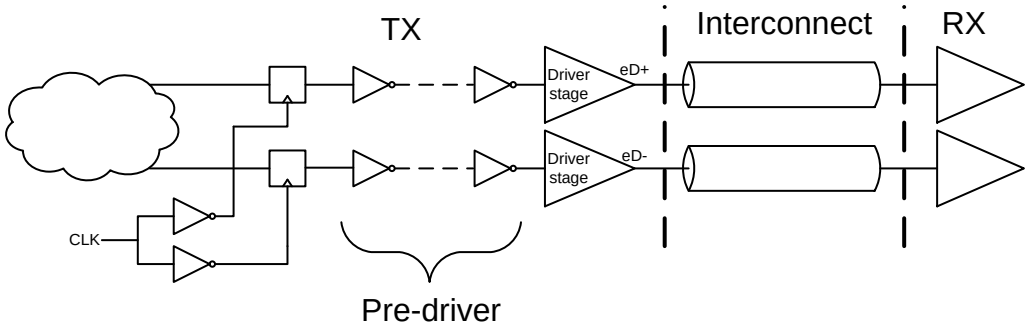


Figure A-1: eUSB2 Driver and Interconnect

- Total skew: 340ps
  - Total driver induced skew=270ps.
    - Main driver induced skew=50ps + 60ps due to mismatch (+/- 3 sigma)=110ps.
    - Pre-driver + Clock path skew + mismatch = 100ps + 60ps = 160ps.
  - Interconnect skew = 70ps (176 ps/inch FR4; or 70 ps/cm); Assuming 1cm mismatch in the trace for 20cm trace width.
- The rise and fall times must be between 0.8ns and 10ns and matched to within max 25%.
  - Case 1: eD+ rise @8.25ps & eD- rise @10ns.
  - Case 2: eD+ rise @800ps & eD- rise @1ns.
- Additional 160ps guard band assumed in current specification